Frequency Analysis of Pulse-Width Modulation on All-Digital Transmitters

Vinícius C. Figueira, Tiago O. Costalonga, Victor Fernandes, Jorge V. de Almeida, Tadeu N. Ferreira, Vanessa P. R. Magri

***Abstract*—This work investigates the frequency spectrum in the modulator and up-conversion outputs of a generic all-digital transmitter architecture. Considering the modulator is implemented as a pulse-width modulation (PWM), it is verified that this up-conversion process introduces a series of impulses resembling the spectrum of a unipolar return-to-zero (RZ) waveform in addition to the PWM impulses. Simulations show the minimum bit resolution of PWM signals where the impulses introduced are almost unnoticed, thus their influence is not distinguished from random background noise. An all-digital transmitter is designed on a field-programmable gate array to verify it experimentally. Experimental results show that reducing power from PWM harmonics leads to a power increase in the RZ harmonics, and vice-versa. These harmonic's power present an energy trade-off relation, a novelty demonstrated in this paper. Finally, but not least, it is observed that filtering the carrier wave out causes a considerable amount of power to be lost.**

***Index Terms*—all-digital transmitters, pulse-width modulation, up-conversion, return-to-zero.**

I. Introduction

TELECOMMUNICATIONS devices highly depend on analog components, limiting the operation of transceivers to a single communication standard historically. Different values of bandwidth and carrier frequency are only achieved by performing significant changes in the components of the transceiver or by designing new ones. To tackle these limitations, digital circuits have been investigated in the literature [1], [2].

Driven by its miniaturization over the last few years, digital circuits may impact a variety of electronic circuit designs, especially in the substitution of analog components in the transmitter or receiver side of radio frequency (RF) systems. This was reinforced by the development of programmable logic devices (PLD), which consist of digital logic circuits capable of being reprogrammed, hence bringing more flexibility to the communication system.

In this context, software-defined radio (SDR) can be designed to be a reprogrammable transmitter, with its structure and operation being specified by software means rather than hardware [3]. A possible way to implement SDR is the all-digital transmitter (ADT), mostly based on a type of PLD called field-programmable gate array (FPGA). By employing an FPGA, it is possible to design a transmitter in which the entire path from the baseband processing until as close as possible to the antenna is digital [4].

Recent works about ADT have focused on improving the flexibility of the carrier frequency in digital transmitters [5], enhancing their capacity to transmit multi-band signals [6]–[8] or reducing hardware consumption [9]–[11], while improving some figures-of-merit, achieving higher values of signal-to-noise ratio (SNR), lower values of error vector magnitude, and higher coding efficiency. These improvements are made by reducing spectral power dispersion from the output signal and, by implementing digital signal processing (DSP) techniques that turn ADTs into even more complex prototypes.

In ADTs, the modulator is typically used to reduce the quantized word from the communication source to a two-level representation. In this sense, PWM is widely adopted, however, it introduces a sequence of harmonic impulses in the spectrum of the transmitted signal [12]. Moreover, the digital up-conversion process emulates the signal multiplication with a carrier, as done by analog systems. In ADTs, the carrier is mapped into a unipolar return-to-zero (RZ) wave, thus another sequence of harmonic impulses is introduced into the spectrum of the transmitted signal. Unless otherwise stated, the RZ referred in this work is the unipolar RZ, where the voltage can only be positive and zero levels [13].

A transmitter employing a 7-bit PWM was developed by [14], where its novelty is the use of a random pattern generation block after the modulator. This proposal intended to change the PWM waveform arbitrarily in order to distribute the energy over the spectrum, relaxing filtering requirements. Using a similar approach to spread the PWM harmonic content, [15] developed a 6-bit PWM-based ADT with a specific mapping process (where a varying PWM duty-cycle is distributed over the wave period), resulting in a carrier power improvement and lower noise influence from other harmonics. This would lower processing requirements from the transmitter, since the random pattern generation block is not used, but the harmonics influence is higher than in the previous case. With the intent to dynamically change the

Vinícius C. Figueira, Tiago O. Costalonga, Victor Fernandes, Tadeu N. Ferreira and Vanessa P. R. Magri are with the Department of Telecommunications Engineering, Federal Fluminense University, Niterói, Brazil, e-mails: viniciuscorrea@id.uff.br, tiago_ogioni@id.uff.br, fernandesvictor@id.uff.br, tadeu_ferreira@id.uff.br and vanessamagri@id.uff.br, ORCID: 0009-0002-8527-8150, 0000-0001-5967-7719, 0000-0001-5179-0645, 0000-0002-9964-9699 and 0000-0002-8151-215X.

Jorge V. de Almeida is with the Electrical Engineering Department, Polytechnique Montréal, Montréal, Canada, e-mail: jorgevirgilio21@gmail.com, ORCID: 0000-0002-7720-2466.

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carrier frequency value, [10] provided an ADT where the PWM modulation and upconversion are performed by a single look-up table (LUT); thus, updating the LUT would rapidly change the carrier. These previous approaches were the main ones in deploying an ADT performing the modulation with PWM.

Most works employ delta-sigma modulation (DSM), proposing different ways to suppress harmonic content. This happens because DSM is capable of achieving better signal-to-noise ratio values, but at the cost of lower sampling rates. To overcome this limitation, ADTs employing polyphasic DSM with multiple cores were proposed [7], [16], [17], but it had a considerable hardware consumption. One proposal is to use hardware reduction techniques in the DSM modulator while keeping a high sampling rate [9]. Moreover, [8] has proposed a 4-bit delta-sigma modulator to reduce the in-band noise and an additional noise shaping (ANS) block to reduce also the noise between multiple bands.

In this paper, we do not propose a new transmitter architecture or improve an existing transmitter. Our goal is to observe a physical phenomenon that occurs between the modulation and up-conversion stages. More specifically, the aim is to verify if there is an energy trade-off between both stages. To demonstrate it, simulations to study the harmonic impulses introduced throughout different bit resolutions of PWM signals are made. These simulations aim to find the minimum bit resolution of PWM signals in which these impulses cannot be distinguished from the background noise. The referred bit resolution that minimizes the unwanted PWM harmonic content are implemented in an FPGA. With this experimental setup, it is expected that only the RZ wave harmonics would be present in the spectrum of the transmitted signal, then their influence on the transmitted signal can be evaluated.

Our simulation and experimental results show that reducing PWM harmonics power implies an increase of the RZ harmonics, demonstrating an energy trade-off between both waves. The main contribution of this paper is to enlighten that the attempts to reduce modulator harmonic power do not imply that the transmitted signal energy use is reduced since it would increase RZ harmonics power. Therefore, filtering the RZ harmonics out causes a considerable amount of energy to be lost.

The remainder of this work is organized as follows: Section II describes the mathematical formulation of the transmitter, Section III shows the simulations performed, Section IV discusses the experimental results and analyses, while Section V brings conclusions and proposes improvements in future ADT projects.

II. Mathematical Formulation

The block diagram of the transmitter developed for the current work is shown in Fig. 1. This architecture of ADT is based on the implementations of [14] and [15], but we do not implement the improved PWM mapping and polyphase with random pattern generation approaches, specified by the respective works. The transmitter developed for this work uses a standard PWM mapping (which is detailed latter in this section) and up-conversion technique proposed by the specified works. It is noteworthy that this work employs a baseband ADT, thus up-conversion stage is implemented after the modulator. The ADT is composed of three main stages: communication source, modulator, and digital up-conversion. According to Fig. 1, memory blocks represent the communication source storing random integer values; the modulator reduces the quantization level of the communication source data to one bit, thus a two-level representation; the digital up-conversion process reorders bits as resembling a carrier multiplication, and serializes them [4]. Moreover, phase-locked loops (PLL) are used to multiply or divide the FPGA embedded clock frequency so that different components of the ADT can have the appropriate frequency of operation. Each stage are introduced as follows.

The first stage is the communication source, which delivers a random quantized word with a length of M bits to the modulator in both direct and quadrature components for each clock step. The communication source (CS) is assumed to be a random variable which follows a discrete uniform distribution, i.e., $CS \in \{0, 1, 2, \ldots, 2^M - 1\}$, in which each word has the same probability of $\frac{1}{2^M}$ to be the input data of the next stage.

The second stage comprises the modulation process, i.e., PWM, which aims to reduce the quantization word from 2^M quantization levels to a 2-level representation. The PWM implementation consists in a mapping process [4], in which the modulator receives M bits from the communication source, and the duty cycle is defined according to the magnitude of the input word. Tab. I shows the PWM for $M = 3$, also referred as a 3-bit resolution PWM signal. It can be seen that if the input word is 5, so the output word is given by $[11111000]$. While the communication source generates M bits for each in-phase (I) and quadrature (Q) component, both PWM modulators generate a single output word with a total size of 2^{M+1} bits.

Tab. I: PWM mapper for $M = 3$.

Word \Bit	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0

The last stage is the up-conversion process (composed by the "Select and Combine" and serializer blocks) consisting of shifting the frequency of the modulated wave to the desired carrier frequency, f_C. Similarly to analogical systems, the frequency shifting is performed by the multiplication of the message signal with the carrier one. Since multiplier blocks in high frequency rates would demand high processing from the transmitter, the frequency shifting can be simplified as a bit reordering procedure performed by the "Select and Combine" as shown by [4].

It is important to verify that the up-conversion involves a bit reordering as $[X_I X_Q \overline{X_I}\ \overline{X_Q}]$, where X denotes the output signal from the pulsed modulator and its subscript denotes the in-phase or quadrature components (I or Q). This reordering

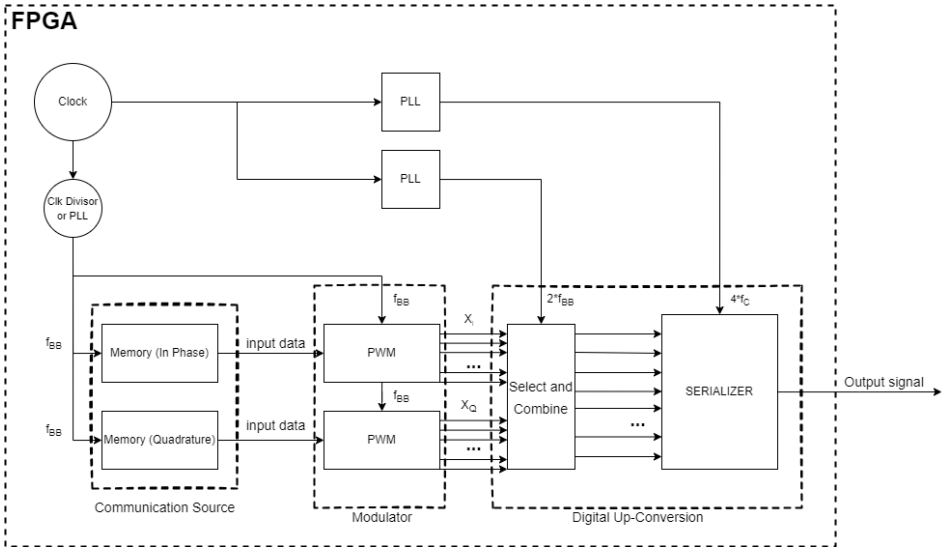

Fig. 1: Block diagram of the ADT employed in this work.

consists of a return-to-zero (RZ) wave since the first two signals are unchanged, and the remaining two are inverted, thus generating a square sinusoidal pattern. This is applied on the "Select and Combine" block, where the PWM wave for the I and Q components are inputs of the block.

The two waves are related since "Select and Combine" emulates the multiplication operation between the PWM and the carrier, the bit word reordering makes the carrier an RZ wave. One property of the Fourier transform for continuous signals is that the multiplication of two signals in the time domain is equivalent to the convolution of their spectrums. This can be verified with a mathematical approximation (considering a constant PWM duty cycle) and analysis.

According to [4], ADTs that employ PWM modulation have its spectrum composed by a series of harmonic impulses. Two parameters determine the frequency spacing between the impulses: the first is the carrier frequency (f_C), and the second is the bit resolution (M) of the PWM signal. For each clock step of the "Select and Combine" block, the sequence of 2^{M+1} bits are serialized with the frequency of $4f_C$, and, thus the frequency range between the impulses is determined by

$$f_{BB} = \frac{4f_C}{2^{M+1}}. \tag{1}$$

The frequency spacing f_{BB} is a consequence of the desired carrier frequency and bit resolution used for the PWM signal, and it is the rate in which the communication source will introduce data to the transmitter. For a f_{BB} clock step, all the bits introduced to the transmitter are mapped for the PWM modulator, serialized in the up-conversion stage and transmitted until the next f_{BB} clock step, as described in equation (1).

Considering $f(t)$ as the mathematical representation of the PWM wave, thus

$$f(t) = \sum_{k=-\infty}^{\infty} A\,\mathrm{rect}_{\mathrm{t_{on}}}\left(t - kT - \left(\frac{t_{on}}{2}\right)\right),$$

where A is the amplitude, t_{on} is the time where the wave remains in the logical level "high", T is the period of the wave, k is the index of the sum and $\mathrm{rect}_{\mathrm{t_{on}}}()$ is the rectangular function of width t_{on}. The duty cycle of the wave is assumed to be $\frac{t_{on}}{T}$. By calculating the Fourier series of $f(t)$, one can find:

$$\overline{f}(t) = \frac{At_{on}}{T} + \sum_{n=1}^{\infty}\Big(\frac{4A}{n\omega_0 T}\Big)\sin\Big(n\pi\frac{t_{on}}{T}\Big)\cos\Big(2n\pi\Big(\frac{t}{T} - \frac{t_{on}}{2T}\Big)\Big), \tag{2}$$

in which its Fourier transform is given by

$$\begin{aligned} F(\omega) = {} & \frac{2\pi At_{on}}{T}\delta(\omega) + \sum_{n=1}^{\infty}\frac{4A}{n\omega_0 T}\sin\Big(n\pi\frac{t_{on}}{T}\Big)\times \\ & \times\pi\Big(\delta\Big(\omega + n\omega_0\Big) + \delta\Big(\omega - n\omega_0\Big)\Big)e^{-j\omega\frac{n\pi t_{on}}{T}} \end{aligned} \tag{3}$$

with $\omega_0 = \frac{2\pi}{T}$ and "$\times$" is the multiplication operator.

Based on (3), it is evident that for every multiple of $\frac{1}{T}$ there will be an impulse component on the spectrum. Since the frequency in which the PWM block operates is $f_{BB} = \frac{1}{T}$, considering the same carrier frequency f_C, higher bit resolutions of the PWM signal would imply in a lower distance between impulses because f_{BB} would be lower as well.

Now, doing the same calculations for the RZ wave

$$g(t) = \sum_{m=-\infty}^{\infty} A\,\mathrm{rect}_{\frac{T'}{2}}\left(t - mT - \frac{T'}{4}\right) \quad ,$$

and

$$\overline{g}(t) = \frac{A}{2} + \sum_{n=1}^{\infty}\frac{2A}{n\omega_0' T'}\big(1 - \cos(n\pi)\big)\sin(n\omega_0' t) \quad , \tag{4}$$

where T' is the period of the wave and n is the index of the sum. Then, its Fourier transform $G(\omega)$ can be obtained as

$$\begin{aligned} G(\omega) = {} & \pi A\delta(\omega) + \\ & + \sum_{n=1}^{\infty}\frac{2A}{n\omega_0' T'}\big(1 - \cos(n\pi)\big)j\pi\big(\delta(\omega + n\omega_0') - \delta(\omega - n\omega_0')\big) \quad , \end{aligned} \tag{5}$$

in which $\omega_0' = \frac{2\pi}{T'}$ and $f_C = \frac{1}{T'}$. Observing $\overline{g}(t)$ and $G(\omega)$, it is verified that all even multiples of $\frac{1}{T'}$ will be null, with only odd components contributing to the spectrum.

A spectrum preview of the output of the ADT can be obtained by means of (3) and (5). The PWM wave spectrum comprises impulses spaced by f_{BB}, and the RZ wave is composed of impulses spaced by odd multiples of f_C.

III. Simulations

Simulations on MATLAB® and Simulink® software were performed to validate the ADT project. This allows to preview the generated waveform in the time and frequency domains.

A. Simulink® Simulations

The spectrum at the output of the ADT is expected to be the convolution of both the PWM and RZ waves. To verify this statement, both spectrums at the output of the PWM modulator (for $M = 6$) and at the output of the "Select and Combine" blocks were plotted, shown for $f_C = 2.5$ GHz by Figs. 2 and 3, respectively.

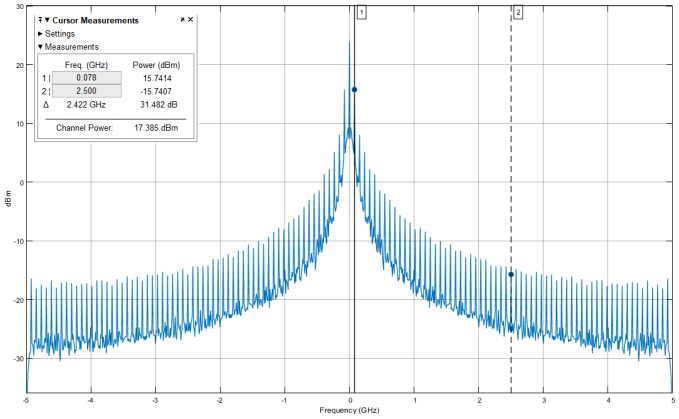

Fig. 2: Spectrum at the output of the PWM block. Harmonics are spaced by $f_{BB} = 78.125$ MHz.

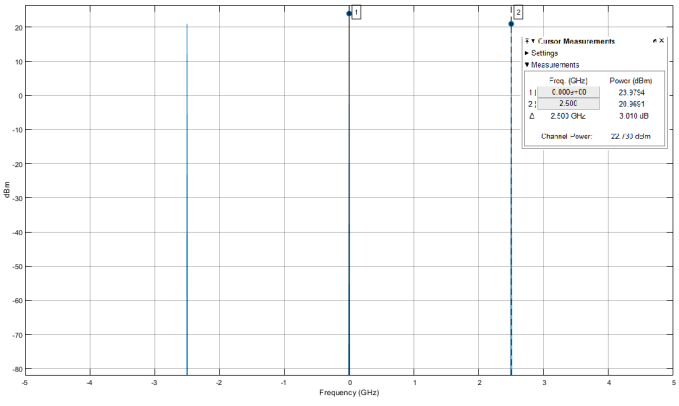

Fig. 3: Spectrum at the output of the Select and Combine block. Impulses are spaced by 2.5 GHz from each other.

Both spectrums shown in Figs. 2 and 3 correspond with (3) and (5), respectively. Furthermore, the spectrum at the output of the ADT is shown in Fig. 4. It can be observed that the resulting spectrum of the transmitted signal from the ADT is the convolution of both spectrums of the waves at the output of the modulator and "Select and Combine" blocks.

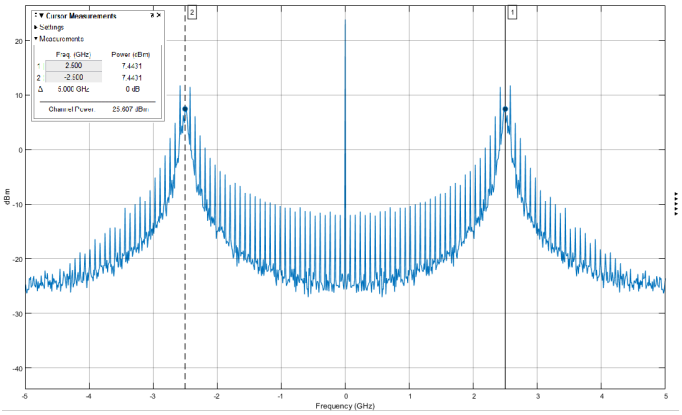

Fig. 4: Spectrum at the output of the ADT.

As observed from the analysis, the spectrum of the transmitted signal is composed of two series of impulses, one originating from the PWM wave and the other from the RZ wave. Most works develop techniques that disperse the power of PWM impulses aiming to concentrate most of the power on the frequency of the carrier, i.e. f_C. Thus, ignoring the spectral components of the RZ wave, which still have a considerable amount of power. The generation of harmonics which are odd multiples of f_C in the spectrum was previously mentioned by [18], [19], where it is only stated that the harmonics, with exception of the first one, i.e. at f_C, are removed by an RF reconstruction filter or a low pass filter.

An analysis to be made is on the importance of the RZ impulse harmonics to the integrity of the transmitted signal. This can be verified experimentally by reducing the presence of the PWM harmonics. One way to do this is by increasing the bit resolution of the PWM signal, because the higher resolution used, the lower is the power of harmonic impulses. Therefore, the influence of RZ wave on the up-conversion process can be further analyzed.

The next set of simulations aims to verify the minimum PWM signal bit resolution where its impulse harmonics are not noticed. In other words, the case where the harmonics power is close to the random background noise.

B. MATLAB Simulations

The second set of simulations regarding the PWM-based ADT performed at MATLAB® served as a way to understand the frequency behavior of the referred modulator, as well as how it changes with the input word size (2 bits, 3 bits, 4 bits, and so on). This allows the confirmation that the previous results obtained in Simulink® apply to different resolutions of PWM modulator.

All simulations are performed for a time execution of $10\mu s$. Considering different values of M for $f_C = 2.5$ GHz, Fig. 5 shows the output spectrum of the ADT from $M = 3$ to $M = 6$, and Fig. 6 shows from $M = 7$ to $M = 10$. Based on the plots

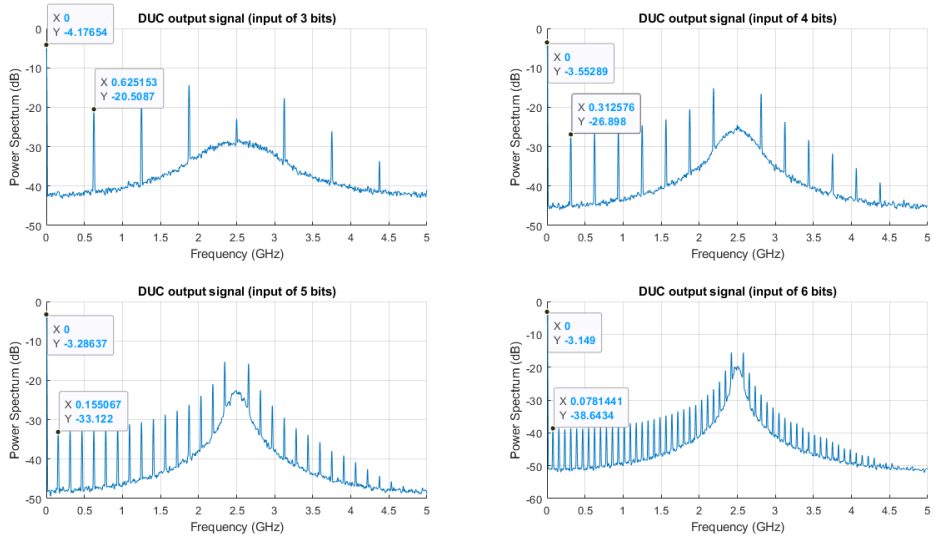

Fig. 5: Transmitted signal power spectrum for $M = 3$ (upper left), $M = 4$ (upper right), $M = 5$ (lower left) and $M = 6$ (lower right).

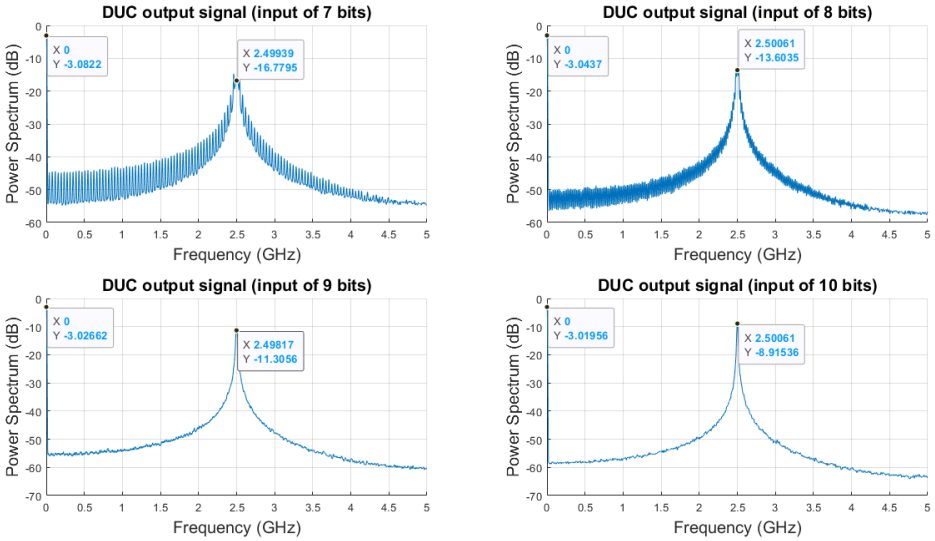

Fig. 6: Transmitted signal power spectrum for $M = 7$ (upper left), $M = 8$ (upper right), $M = 9$ (lower left) and $M = 10$ (lower right).

displayed, it is notable that the impulses are spaced by f_{BB} and that they are multiples of the baseband frequency.

It can be observed that the impulse at the main frequency (i.e., 2.5 GHz) tends to concentrate more power with the increasing resolution of the PWM modulator. It is important to note that f_{BB} reduces with constant f_C and increasing the bit resolution of the PWM signal, as demonstrated by (1). As well, both impulses and noise-floor powers are reduced by increasing the bit resolution of the PWM signal. When $M = 3$, $M = 6$, and $M = 10$, the lowest-frequency harmonic component had approximately -20 dB, -40 dB, and -60 dB of power, respectively.

It is noteworthy that starting from the 9-bit resolution PWM, the impulses are not distinguished from the background random noise since their power is approximately the same as the noise floor. Performing an experimental setup using the 9-bit PWM would be sufficient for the analysis of the ADT output spectrum with only RZ impulses.

Notably, from Figs. 5 and 6, one can see the presence of a considerable amount of power in the DC component of all spectrums for each bit resolution of PWM. This is clearly expected, as shown in (5), since there is a Dirac delta function, as a consequence of employing a unipolar RZ carrier for up-conversion. One straightforward way to suppress this DC component is to employ another line code which does not generate it, such as the polar RZ [13]. In this case, the

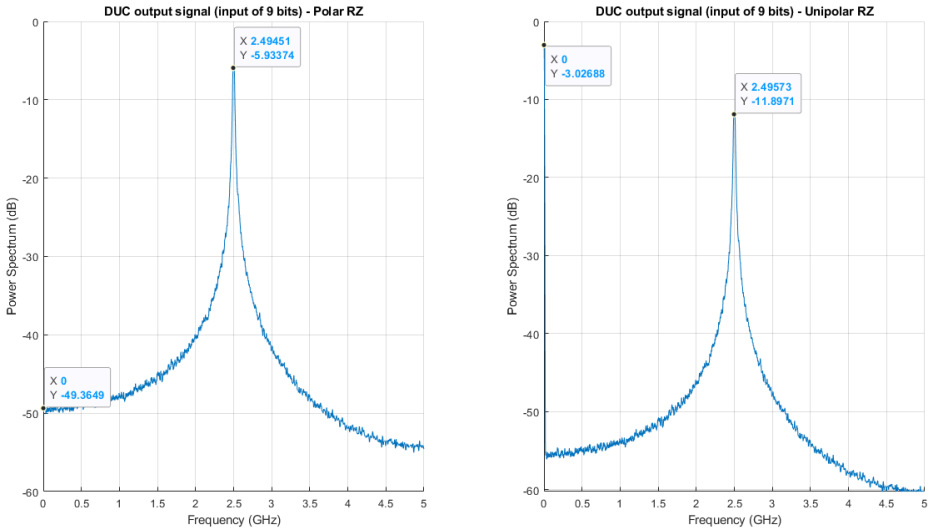

Fig. 7: Transmitted signal power spectrum for 9-bit resolution PWM with the use of a polar RZ line code (left) and a unipolar RZ line code (right).

polar RZ considers that the positive level will always return to the negative (instead of zero) level. Fig. 7 shows the output spectrum of the ADT with $M = 9$, when polar RZ (left) and unipolar RZ (right) are used for the up-conversion stage.

From Fig. 7, it is clear that the DC component was suppressed and the carrier increased its power for the polar RZ. However, the implementation of polar RZ in FPGA would also require a level-shifter circuitry, which is out of the scope of the current work.

In the following section, two experiments are performed, where the first one considers a 4-bit PWM signal and the second one a 9-bit, and both have the same carrier frequency of $f_C = 500$ kHz. The results are compared, where it is expected that the main difference is the presence of the PWM impulse harmonics.

IV. Experimental Setup and Results

The transmitter is prototyped according to the FPGA in which it was implemented. To this work, the FPGA DE10-Lite model from Altera®/Intel® is used to validate the transmitter prototype. Arduino I/O ports are used instead of SMA connectors, and a multiplexer is programmed to replace the MGT and perform the function of the serializer.

Fig. 8 shows the experimental setup used. The materials used for the experiment are listed below.

- FPGA Intel® MAX 10 (kit DE10-Lite);
- Male-male jumpers;
- Alligator connectors;
- Rigol DSC1302CA scope;
- Anritsu MS2034A spectroscope;
- Connectors for the scope and the spectrum analyzer;
- Software Quartus-Prime version 21.1.

In the experimental setup, a male-male jumper is connected to one of the FPGA I/O port, while another male-male is connected to a ground port. Alligator connectors are used for both scope and spectroscope connections with the male-male jumpers. An additional junction should be used for the spectroscope to support the alligator connectors. The ADT code is implemented using Verilog HDL in Quartus-Prime software.

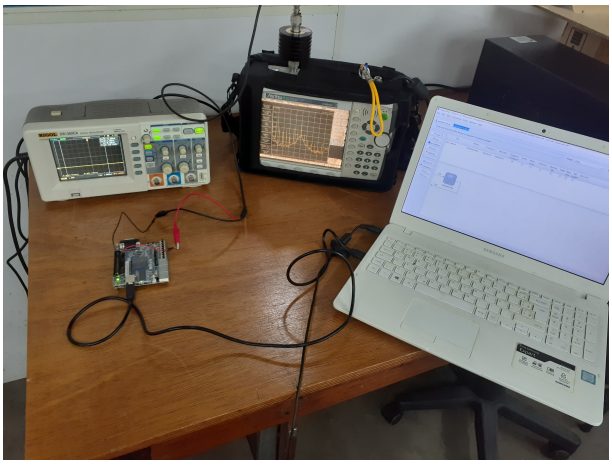

Fig. 8: Experimental setup with the Rigol DSC1302CA scope (on the left) and Anritsu MS2034A spectroscope (at the center).

To verify how the PWM impulses influence the signal spectrum, the ADT is configured to operate with $f_C = 500$ kHz and $M = 4$. Thus, by means of (1), one can find $f_{BB} = 62.5$ kHz. The choice for a low carrier frequency $\left(f_C = 500 \text{ kHz}\right)$ is made, since the MAX10 FPGA do not support frequencies in GHz range (the maximum frequency it supports is 400 MHz) and also because the male-male jumpers have a selective behavior for frequencies above MHz range. The results obtained can be verified for higher frequencies if deployed on a appropriate FPGA with SMA connectors and GHz frequency capabilities.

Fig. 9 shows the wave generated by the ADT in the time domain, measured by a Rigol DSC1302CA oscilloscope. The wave obtained was rectangular, like an RZ wave, but with some discontinuities caused by the PWM duty cycle changes. The discontinuities cause a slight change in the frequency measured by the scope.

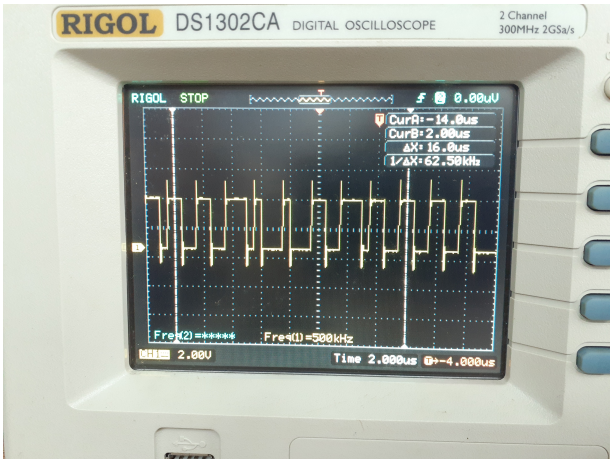

Fig. 9: Output signal obtained for $f_C = 500$ kHz.

With a well-defined square waveform in time, it is possible to verify the characteristics of the spectrum that compose it. The Anritsu MS2034A spectrum analyzer is used and generates a well-defined spectrum, as shown in Fig. 10 with 1 MHz of frequency band being displayed. One can observe that the central frequency is 500 kHz and that its spectrum is accompanied by a series of harmonics that repeat at each multiple of the baseband frequency of 62.5 kHz. A second marker, depicted in red, is added at a harmonic adjacent to the central component of the spectrum, evidencing its frequency of 436.6 kHz, which is approximately spaced by f_{BB} from the carrier frequency f_C.

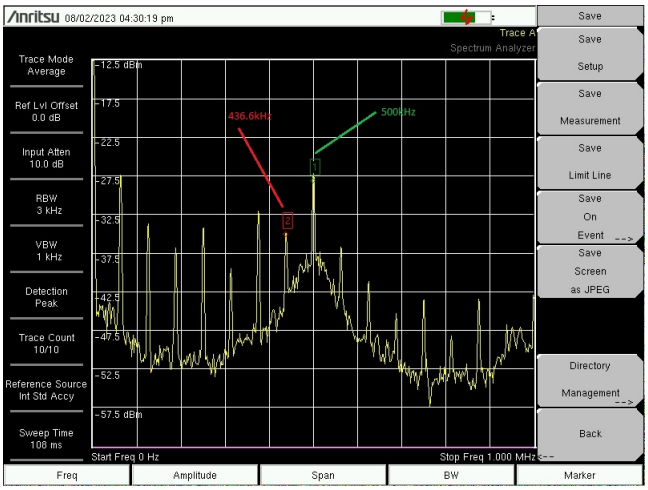

Fig. 10: Spectrum of the output signal with 500 kHz.

To verify the other sequence of impulse harmonics, introduced by the RZ wave, the spectroscope was configured for a wider spectrum view with 3 MHz of frequency band being displayed as shown in Fig. 11. The RZ impulse component can be observed at every odd multiple of 500 kHz; the even multiples are notches, as verified from Equation (5). The RZ harmonic impulses carry a considerable amount of power: the difference between the first and third impulse components is approximately 10 dB, while the difference between the third and fifth ones is around 5 dB.

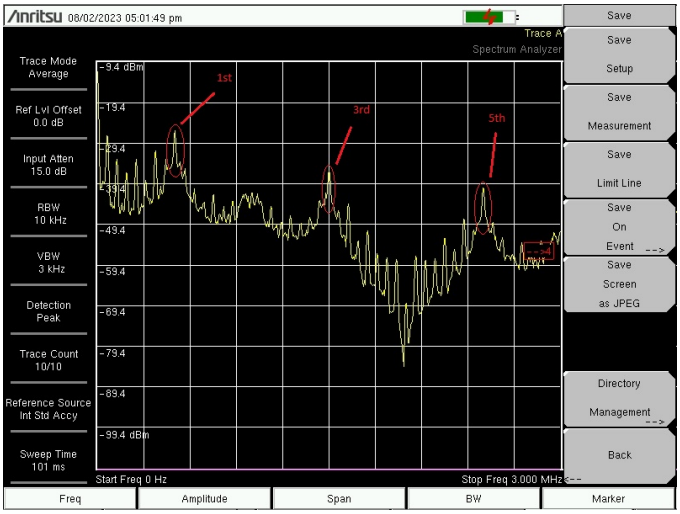

Fig. 11: Wide spectrum of the signal with $f_C = 500$ kHz and $M = 4$.

With the simulation results from Fig. 6, we expect that $M = 9$ would be the lowest resolution where PWM harmonics influence would not be significant to the transmission of the signal. From this analysis, a second experiment was performed, considering a PWM modulation with $M = 9$. Maintaining the same carrier frequency $f_C = 500$ kHz, according to (1), $f_{BB} = 1.953$ kHz. To capture the RZ harmonics spacing, the same frequency band from 0 Hz to 3000 kHz was set, as shown in Fig. 12.

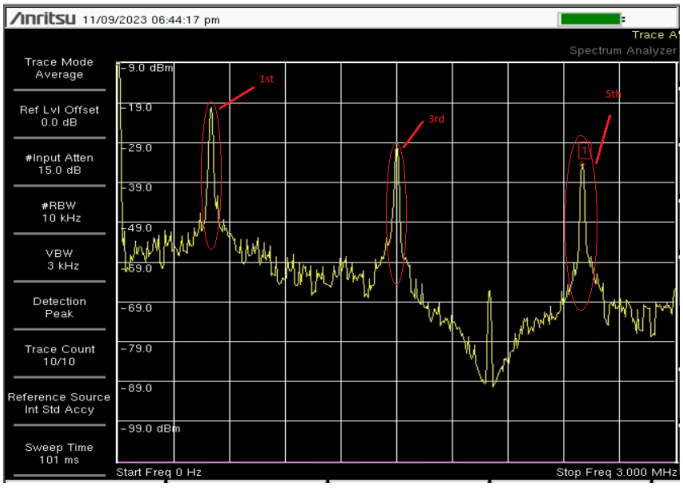

Fig. 12: Spectrum of the signal with $f_C = 500$ kHz and $M = 9$.

From Fig. 12, two analyses can be made. First, comparing it with Fig. 6 with $M = 9$, one can see that the PWM harmonics still exist, but they do not remain static. During

runtime execution, the random noise interferes with them, making them alternately fade in and out. This confirms that although the PWM harmonics are not totally dispersed, they are not easily distinguished from the noise floor. The second analysis shows that comparing Fig. 12 with Fig. 11, the RZ harmonics have their power increased significantly by almost 10 dB, which is also verified in Fig. 6 when observing the RZ impulses power throughout different bit resolutions of PWM signals.

It is important to emphasize that PWM harmonic peaks power decreases throughout increasing bit resolutions of PWM, but this spectral power is not lost at all; it is concentrated in RZ harmonics. This happens because the transmitted signal from the ADT behaves similar as an RZ wave in the time domain, its discontinuities mark the PWM positive-edges and negative-edges transition, and those discontinuities tend to be more rare with higher bit resolutions of PWM signals [20]. This means that there is a trade-off between the PWM harmonics spectral power and RZ harmonics spectral power; lowering PWM peak power concentrates more power in RZ peaks, thus fitering still remains a challenge. In other words, if the odd RZ harmonics are filtered out, a considerable energy loss will be observed.

V. Conclusions and Perspectives

A PWM-based ADT is created to verify the time and frequency domains of the generated wave from the communication source and how it changes throughout the transmitter for different bit resolutions of PWM signals. A mathematical formulation of the wave processing by the PWM and up-conversion blocks is done, showing that it is composed of harmonic impulses spaced by baseband and carrier frequencies. Simulations made on MATLAB® tested the PWM throughout increasing bit resolutions, the results show that the 9-bit PWM signal is the minimum where PWM harmonics cannot be distinguished with the noise floor.

The PWM-based ADT design is implemented in the MAX 10 FPGA. Considering setups for PWM with bit resolutions 4 and 9 employing the carrier frequency of 500 kHz, the results show that the PWM harmonic suppression would lead to an increase in RZ harmonics spectral power, as a trade-off between both. Suppress PWM harmonics increase spectral power for the first RZ harmonic (or the carrier), however filtering would remain a challenge since a considerable amount of power would be lost with the odd RZ harmonics.

A proposal that can be made for future works in ADTs is to use other line codes rather than unipolar RZ for the up-conversion process (in the "Select Combine Block") that can also emulate the carrier multiplication. The polar RZ showed to be an interesting alternative for avoiding wasting energy with the DC component. Most line codes have a well-known spectrum, thus the one with less power in its harmonics over the first one would be more appropriate than the RZ. This proposal, in combination with the use of a higher bit resolution PWM (such as ninth or tenth), would optimize the power concentration in the first multiple of the carrier frequency. This implementation would fit applications that do not rely on high throughput and that use frequencies in the hundreds of MHz range, since it would require less hardware complexity and clock requirements. This compensates the logical resource usage from the FPGA (or PLD) introduced by the PWM.

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Vinícius Corrêa Figueira acquired the bachelors degree in Telecommunications Engineering from the Federal Fluminense University (UFF), Brazil, 2023. His major interests are related to communication systems and FPGAs.

Tiago Ogioni Costalonga is a Brazilian Navy's Officer, graduated in Electrical Engineering by Universidade Federal de Viçosa (UFV), pos-Graduated in Weapon Advance System by Pontifícia Universidade Católica do Rio de Janeiro, and Master degree in Telecomunication Engineering by Universidade Federal Fluminense. His research interest include radar, robotics and computar programming.

Victor Fernandes received the D.Sc. degree in Electrical Engineering from the Federal University of Juiz de Fora (UFJF), Brazil, in 2021. Since 2021, He has been an Assistant Professor at the Department of Telecommunications Engineering at the Fluminense Federal University (UFF), Brazil. His research interests include signal processing, wireless communication, power line communication, energy harvesting, radar detection, and 5G.

Jorge Virgilio de Almeida received the D.Sc. degree in electrical engineering at the École Polytechnique de Montréal, Montreal, QC, Canada. His current research interests include power amplifiers, metamaterials, near-field and far-field simultaneous wireless power and information transmission systems for massive Internet of Things (IoT), printed antennas, and seamless integration of circuits.

Tadeu N. Ferreira He is a D.Sc. in Electrical Engineering at UFRJ in 2009, with a post-doc in UFRJ in 2010. Currently, he is an Associate Professor at UFF. He is the author of 23 articles published in journals. He has advised 1 doctorate thesis and 22 master dissertations.

Vanessa Przybylski Ribeiro Magri Electrical Engineer with an emphasis on Telecommunications, she completed her D.Sc. degree at PUC-Rio in 2011. She completed her Post-Doctorate in a Project linked to the National Institute for Space Research (INPE), the National Institute of Science and Technology, CETUC-PUC-Rio and the National Institute of Space Technologies. She began her career as a professor at the Department of Telecommunications Engineering (TET) at UFF (Universidade Federal Fluminense) in 2013. She currently works as coordinator of LAPROP (UFF Antennas and Propagation Laboratory).