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2D-FDTD Electromagnetic Simulation of an Ultracompact All-Optical Logic Gate Based on 2D Photonic Crystal for Ultrafast Applications

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***Abstract*—In this paper, the concept of photonic crystals (PhCs) is fundamental to designing and simulating an all-optical logic gate device. We proposed an all-optical switch composed of two-dimensional (2D) photonic crystal waveguides with a central photonic crystal ring resonator (PCRR). The new all-optical NAND logic gate device comprises two linear waveguides coupled to each other through a single compact PCRR. The plane wave expansion (PWE) and finite-difference time-domain (FDTD) methods are applied to simulate the properties of the system. The structure is implemented on the operational wavelength of 1700 nm on an air wafer of only 12 μm × 12 μm. Indeed, the simulation results show that the proposed all-optical NAND gate is a strong candidate for ultrafast photonic integrated circuits (PICs) for applications in optical communications, being advantageous with high transmitting power, with simple design, and without the use of optical amplifiers and nonlinear materials.**

***Index Terms*—Photonic Crystals, Wave Propagation, Electromagnetic Simulation, All-Optical Logic Gates, Interference Effect, Performance Analysis.**

I. INTRODUCTION

IN today's world, with diversified and rapidly growing technologies, innumerable advancements are needed in every field of research, especially in electronics and communications devices [1]. In this way, we are interested in the context of this advancement form electronics to world of optics.

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First, all-optical logic gates (AOLGs) based on the characteristics of semiconductor optical amplifiers (SOAs) were reported [2], [3], [4]. However, there are some limitations to these methods, among which we can mention the high input power with a low power transmission, complex and expensive projects, in addition to the speed and size of the structures, causing them to be less used, making on-chip integration difficult [4].

Photonic crystals (PhCs) are periodic dielectric nanostructures [5] of diverse alternating layers of specific materials, with different refractive indices, which enable the manipulation and control of various forms of electromagnetic radiation (EMR).

Depending on the structural design, the refractive index varies in one, two, or three directions, resulting in 1D, 2D, or 3D photonic crystals [5]. The 2D photonic crystals are broadly used to design all-optical logic gates.

One of the emerging topics in electronics is increasing the speed of information transfer. For this reason, the design of digital optical devices has become an increasing research focus.

AOLGs based on 2D photonic crystals [5] with small sizes must be designed for high-speed optical integrated circuits, which is the gateway to the design of optical processors [6], [7], [8]. This work is made to design a NAND gate with a small size, and a simple structure that can be used in PICs.

The waveguides of a photonic crystal can have very sharp curves, with low losses in the structure, contributing to an increase of integration density of PICs components by several orders of magnitude [9]. Photonic crystals offer a wide range of applications in ultracompact all-optical integrated circuits with a high reduction in energy consumption. Several logic gates based on 2D photonic crystal platforms have been demonstrated [10].

To recognize the performance of the all-optical logic gates, different structures have been proposed, such as a multimode interference (MMI) [9], Mach-Zehnder interferometers (MZIs) [9], semiconductor optical amplifier [10], [11], among others.

The study of photonic crystals allowed the design of certain structures with interesting optical properties, including the specific frequencies range denoted by photonic band gap (PBG) [5], [12], [13] and that can be calculated using the plane wave expansion (PWE) method [12]-[15]. The light in this range of frequencies does not propagate through this structure [14], [15]. So, the electromagnetic (EM) waves incident with frequencies located in this range are reflected by the crystal. Therefore, the light flux can be controlled [5].

Lately, many researchers have become interested in designing all-optical logic gates from photonic crystals, as it is an essential optical media to form a new generation of optical processors and optical communications systems [8], [16], [17]. Moreover, some of these authors designed logic gates based on linear or nonlinear resonators, where they studied the advantages and disadvantages of each method used. Indeed, several papers have already been published about the AOLGs based on 2D PhC [18], [7], [3], [19], [20], [4].

As was observed in paper [18], several AOLGs of a 2D photonic crystal were designed. These were designed based on MMI, and the OR, NAND, XNOR and XOR logic gates were realized. Such structures are simulated and analyzed via the FDTD and PWE methods. The contrast ratio for OR and NAND logic gates is 13 dB. For XNOR, it was 17 dB, and for XOR, about 21dB in C-Band with the spectral region from 1530 nm to 1565 nm. These AOLGs are potential candidates for constituting PICs, which will be used in all-optical signal processing, all-optical networks, and photonic computing.

Reference [7] presents the design of an all-optical majority logic gate based on photonic crystals. This logic gate has a simple structure in a square lattice, in which the refractive index used for all rods is 3.47. The lack of PCRRs in this design reduces device complexity and size. The FDTD method is used to compute the propagation of optical waves for the different inputs in this structure. In addition, logic ‘0’ and logic ‘1’ are defined based on the amount of power transferred to the output port.

In another study [3], the authors present a device used to obtain AOLGs, based on phase shift keying (PSK) technique and beam interference effect. The working principle is shown through simulations using the FDTD and PWE methods. So, the AND, NOR, OR and NAND logic gates were realized. The minimum contrast ratio is 8.88 and 10.31 dB for all-optical AND/NOR and OR/NAND logic gates, respectively. The minimum bit rate is 3.34 Tbps for AND/NOR and 5 Tbps for OR/NAND logic gates. Due to small size of proposed AOLGs and its clear operating principle, these structures can be used for future applications in PICs.

Reference [19] shows a new approach for the design of AOLGs based on 2D photonic crystals in a square lattice of silicon rods (Si) on silica (SiO_2). It consists of two PCRRs and cross-shaped waveguides without optical amplifiers and nonlinear materials. The structure is simulated and analyzed by the FDTD and PWE methods. The numerical simulation results demonstrate that the structure acts as a NOR and NAND logic gate. The logical levels, high ‘1’ and low ‘0’ are defined. Since this structure is composed of linear material, it presents low power consumption compared to structures composed of nonlinear materials. It is observed that the construction of new structures causes PCRRs to have further applications in ultracompact PICs.

Reference [20] proposed an all-optical structure based on two types of defects: the point defect and the line defect. The defects were created in a square lattice of silicon dielectric rods in contrast to air. The device design features two input ports with two output ports. The operating frequency range of the device is from 0 to 0.45 (a/λ). However, it was adjusted to 0.419 for low dispersion conditions, and the structure is implemented with an operational λ equal to 1.55 μm. Regarding the performance presented after the simulations, the maximum contrast ratio reached was about 6.767 dB. According to the results, the authors reported that the device can act as an XOR and OR logic gate.

It is shown in [4], a trifurcation structured optical logic gates based on 2D PhCs composed of a square

lattice of air holes in silicon. The PWE and FDTD methods are used to analyze the behavior of the structure. Thus, the results obtained prove the functionality of OR, AND, NOR and NAND logic gates. Regarding the performance obtained by the device, specifically for AND, NAND and NOR gates, the contrast ratio was 6.15 dB, 5.79 dB and 2.97 dB, respectively. Furthermore, the bit rate and footprint were calculated for the simulated all-optical logic gates. The footprint for the proposed logic gate was around 424.7 μm. The contrast ratio obtained for the AND and OR logic gates was 6.52 dB and 10.79 dB, respectively.

The works mentioned above are characterized by the use of a numerical methodology to analyze all-optical logic gates. AOLGs are available for various applications [21], [22], [23], for example, in digital processing of optical communications systems, and in manufacturing more complex devices for use in ultrafast photonic integrated circuits.

The numerical simulation has been performed through the 2D FDTD method [24], [25], which simulates electromagnetic wave propagation in any materials in the time domain.

Following the lines of the above citations. We introduce a new design of a very compact structure to be used as a NAND logic gate and simulate it within the FDTD approach, which may contribute to the density of component integration in optical communications systems.

II. Structure Design, Materials and Methods

As shown in Fig. 1, we propose a new structure for an all-optical switch composed of two photonic crystal waveguides (horizontal and vertical) and one central PCRR. This structure realizes the all-optical NAND logic gate based on beam interference effect. In a 2D system, this structure consists of a 19 × 19 square lattice of silicon (*Si*) rods immersed in air background.

The lattice constant, denoted by '*a*', is 0.5943 μm, being the distance between two consecutive rods, as shown in Fig. 1. The radius of the silicon rods is $r = 0.2a$, approximately 0.11886 μm. The relative permittivity of the dielectric rods in the 2D structure is $\varepsilon_r = 12$, which is equivalent to $n = 3.46$ refractive index, where $n = (\varepsilon_r)^{1/2}$.

The structure of the proposed NAND logic gate is formed by a PCRR inside, which was incorporated by the insertion of some defects. The point and line defects created in the PhC structure were made with dielectric silicon rods, which are added or removed from the interior region of the structure in the *x*-*z* plane. The diameter of the PCRR is $d = 6a$.

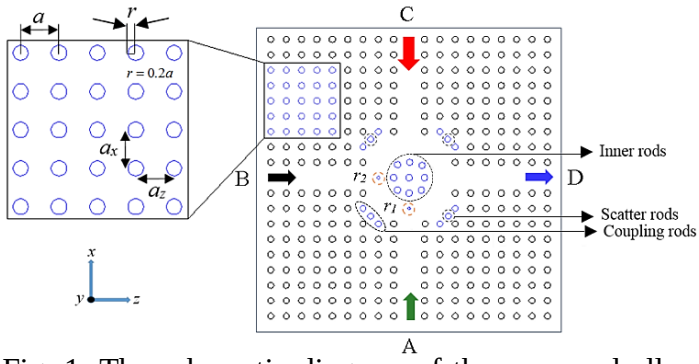

Fig. 1. The schematic diagram of the proposed all-optical NAND logic gate device.

The depicted logic gate in Fig. 2 is analyzed in the *x*-*z* plane on the square lattice composed of silicon rods in the air. The wafer size is only 12 μm × 12 μm.

As shown in Fig. 2, *scatter rods* are shifted from their original position along the *x* and *z* directions of $0.25a$ concerning the original lattice to achieve a circular symmetry and avoid backward reflections due to the curve formed in the central waveguide. The scatter rods are placed at each of the four corners of the PCRR, denoted by s_1, s_2, s_3 and s_4, to improve coupling efficiency.

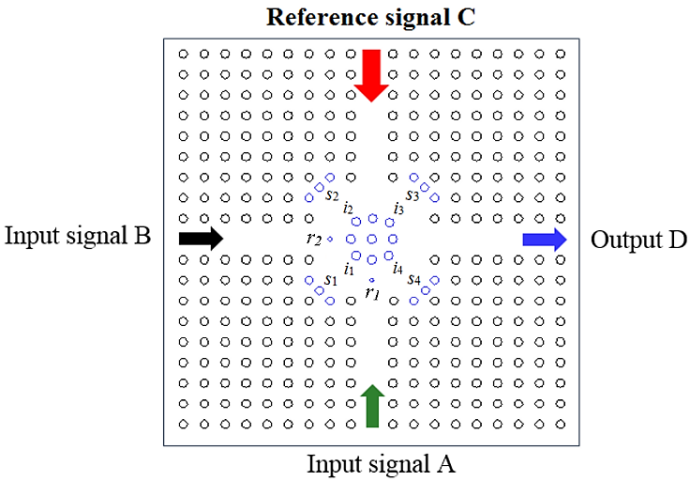

Fig. 2. The simulation scheme for the square silicon structure of the all-optical NAND logic gate.

The rods located in the center of the PCRR are called *inner rods*. As illustrated in Fig. 2, the PCRR is constructed by shifting the adjacent inner rods (i_1, i_2, i_3 and i_4) from their original position along the x and z directions of $0.25a$ with respect to the original lattice.

In Fig. 2, two dielectric rods are added around the inner rods of central PCRR, characterizing specific defects in the horizontal and vertical waveguides, respectively with radius (μm) $r_2 = 0.1a$ and $r_1 = 0.05$, contributing to the NAND functionality. The silicon rod shown in Fig. 2, with a radius r_1 of 0.05 μm, creates a point defect that are responsible for the light confinement property [3], [5]. Tab. I shows the complete set of geometrical parameters of the structure design.

TABLE I
THE DESIGN GEOMETRICAL PARAMETERS OF THE 2D PHOTONIC CRYSTAL STRUCTURE.

Parameters	Materials/values
Wafer	Air
Dielectric material	*Si*
Refractive index	3.46
Wafer size	12 μm × 12 μm
Rod radius 'r'	0.11886 μm
Radius of rod in r_1	0.05 μm
Radius of rod in r_2	0.05943 μm
Lattice constant 'a'	0.5943 μm

In addition, this structure consists of two input ports A and B, one reference port C and one output port D, as shown in Fig. 2.

The NAND structure is excited in reference port C, with control by input ports A and B, and the signal can be verified in output port D.

The optical beams, while confined through the waveguides, obstruct each other, and the transmission of these optical beams depends on the type of interference that can occur.

According to wave optics theory, the constructive interference occurs when two optical beams differ by a phase difference of $2k\pi$ ($k = 0, 1, 2 ...$), and the destructive interference occurs while the two optical beams have a phase difference of $(2k + 1)\pi$ ($k = 0, 1, 2 ...$) [3], [10], [11].

For all binary combinations of the input ports, the reference beam at port C is always applied with a phase of 0°. Thus, as an illustration, when an optical beam is applied at input port A, its phase must be 0° so that constructive interference can occur between the optical input beam and the reference beam, to provide a power signal at output port D.

Specifically, there is always a reference signal switched on the upper, in port C of the vertical waveguide, to guarantee the NAND functionality. Thus, when no optical signal is applied to ports A and B, the signal from the reference port C is the only which reaches the output port D.

There are two types of logic states: high optical power (ON state) and low optical power (OFF state). Indeed, in the ON state, we have logic '1' (or bit 1 or 1), while in the OFF state we have logic '0' (or bit 0 or 0).

There are two thresholds for identifying the logical states, as shown in Fig. 3. A lower threshold means power below this level acts as a logic low or logic '0'. Similarly, power values above the upper threshold act as a logic high or logic '1'. No state is defined between the upper and lower thresholds.

According to Fig. 3, the detected optical power at the output port D is considered as logic '1' if the power is greater than or equal to 0.3, and is considered logic '0' if the power is less than or equal to 0.1. Therefore, the maximum power should be transmitted in the logic '1' state as opposed to logic '0' state.

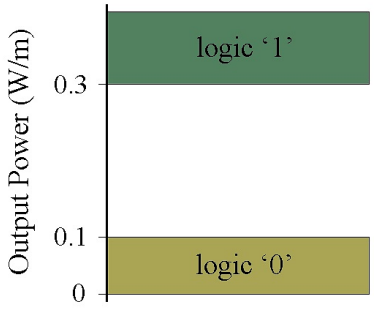

Fig. 3. Definition of '0' and '1' logic levels with the corresponding power values at the output.

The light confinement mechanism of photonic crystal silicon rods provides the switching property between logic '1' and logic '0' of the logic gate.

The numerical simulations of the propagation of electromagnetic waves in planar PhCs structures are characterized using Maxwell's equations [26].

The PWE method [12]-[15] is used to calculate the PBG and propagation modes of the PhC structure, while the 2D-FDTD method is used to calculate the spectrum of the power (in W/m) transmission and field distribution that is based on numerical solutions of Maxwell's equations.

It is assumed that the material is linear, isotropic, periodic with lattice vectors and lossless. Indeed, the Maxwell's equations are given by

$$\begin{aligned} \vec{\nabla}\times\vec{E} &= -\mu\frac{\partial\vec{H}}{\partial t} \\ \vec{\nabla}\times\vec{H} &= \varepsilon\frac{\partial\vec{E}}{\partial t} \\ \vec{\nabla}\cdot\vec{E} &= \vec{\nabla}\cdot\vec{H} = 0 \end{aligned} \tag{1}$$

The FDTD method is based on Yee's algorithm to study the 2D-PhCs because the computational time and memory requirements are reduced [26].

Indeed, in 2D simulations the absorbing boundary conditions in the PhC structure must be considered, which is isolated so as not to experiment with external and internal interference or related to the physical [25], [26] phenomena that occur during the simulations. Thus, the structure is surrounded for the perfectly matched layer (PML) [26], [27]. The PML is used as the absorbing boundary condition (ABC) at the edges of the computational zone.

III. Performance Analysis

In order to analyze the performance of the all-optical NAND logic gate, the parameters such as contrast ratio (*CR*), insertion loss (*IL*), quality factor (*Q*-factor), response time (RT) and bit rate (BR) are used, measured from the output results.

There are two types of logic states: high optical power transmission (ON state) and the low optical power transmission (OFF state).

The contrast ratio is the most important parameter for studying the performance of AOLGs [23]. The contrast ratio [3], [28], [29], [30] is defined as the ratio between the average power in the ON state (P_{ON}) and the average power in the OFF state (P_{OFF}), is given (in dB) by

$$CR = 10\log\left(\frac{P_{ON}}{P_{OFF}}\right) \tag{2}$$

where P_{ON} is the power level of logic '1' (or bit 1) and P_{OFF} is the power level of logic '0' (or bit 0). The switching property between the logic '1' and logic '0' of all-optical logic gate is achieved by the light confinement property of square lattice silicon rods.

Furthermore, the performance of proposed design is also analyzed by finding out insertion loss, based on the obtained values from the simulation results. The insertion loss [31], [32], [33] is calculated by

$$IL = 10\log\left(\frac{P_{OUT}}{P_{IN}}\right) \tag{3}$$

where P_{OUT} is the output power level, and P_{IN} is the input power level.

The quality factor [34], [35], is defined as follows

$$Q = \frac{\lambda_0}{\Delta\lambda} \tag{4}$$

where λ_0 is the resonance wavelength of structure, and $\Delta\lambda$ is the full width at half maximum (FWHM) value of the resonance.

In addition, to study the efficiency of the system, the response time [4] and speed also are calculated [36], being used as a measure of interactive system performance.

Operating speed [3], [36], namely bit rate, can be calculated from response time. Bit rate (in Tbps) is defined as the reciprocal of response time observed. It is a factor of the data transfer speed through logic circuits.

IV. Numerical Results and Discussion

Fig. 4 shows the band diagram of the proposed all-optical structure, based in 2D photonic crystals. The band diagram was calculated by the plane wave expansion (PWE) method.

The PBG is calculated for the Transverse Electric (TE) mode, with the propagation modes in the first Brillouin zone. The first frequency range obtained is given by $0.320267 \leq a/\lambda \leq 0.3924$, corresponding to the wavelength range $1.515 \leq \lambda\ (\mu\text{m}) \leq 1.856$. This range covers the optical communication, C, and L bands. The lattice constant 'a' and the rod radius $r = 0.2a$ have been chosen to achieve a PBG around the operational wavelength $\lambda = 1.7\ \mu$m. To select the operating wavelength, it is considered

$$\frac{\omega a}{2\pi c} = \frac{a}{\lambda} \tag{5}$$

where the left-hand side part denotes the frequency of bandgap. According to Fig. 4, the operational wavelength of 1700 nm falls in the first bandgap. Indeed, this structure can operate at any wavelength within the photonic bandgap, including the telecommunication wavelength of 1550 nm.

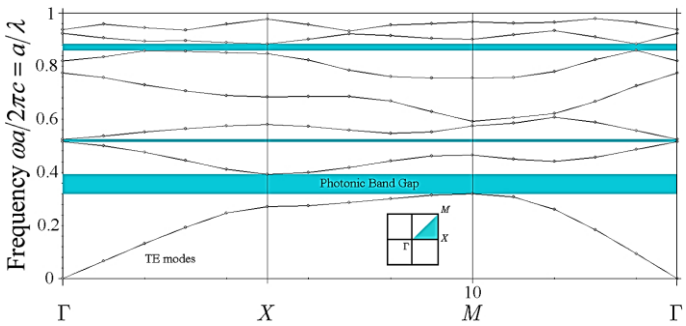

Fig. 4. The band diagram of proposed all-optical PhC structure.

In these simulations, a continuous wave (CW) is designated as the optical source which is functional at the ports of the structure. The NAND Boolean function output is verified by two optical switches operation, an AND gate followed by a NOT gate. The structure is excited at the input ports with a Gaussian light source with the resonant frequency of 0.34958 a/λ, and corresponding wavelength of 1.7 μm, where c is the speed of light in vacuum.

The performance of this device is verified by calculating the contrast ratio for various wavelengths. Indeed, to obtain the operational wavelength, we scanned the wavelength range obtained in the PBG of the structure and calculated the contrast ratio between the logic '0' output power and the logic '1' output power, as shown in Fig. 5. Thus, according to Fig. 5, it is verified that the maximum value of the contrast ratio is 12.04 dB at the operational wavelength of 1.7 μm. Therefore, the operating frequency used in numerical simulations is $\omega a/2\pi c = 0.34958$.

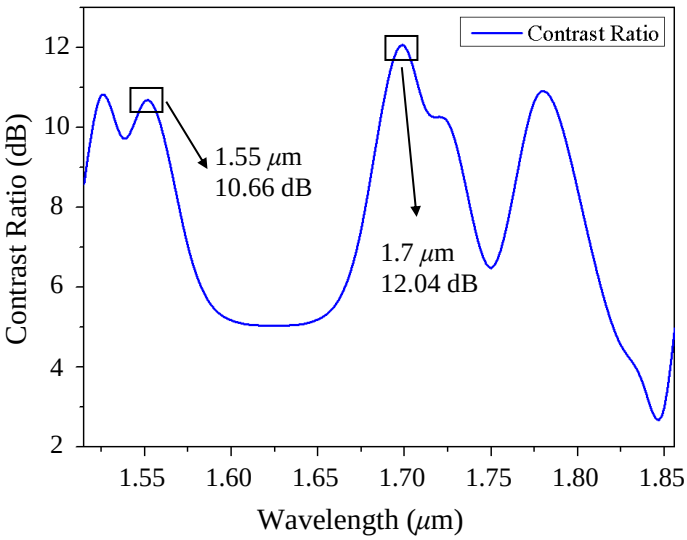

Fig. 5. Contrast ratio curve of the proposed NAND logic gate.

TABLE II
SIMULATION PARAMETERS OF THE NAND LOGIC GATE BASED ON 2D PHOTONIC CRYSTAL STRUCTURE.

Parameters	Values
Wavelength	1.7 μm
Type of Polarization	TE
Input Field Transverse	Gaussian
Number of mesh cells X	244
Number of mesh cells Z	244
Mesh Delta X (μm)	0.049
Mesh Delta Z (μm)	0.049
Signal intensity for logic '0'	0.09 W/m
Signal intensity for logic '1'	1.44 W/m

Tab. II shows the simulation parameters used for the all-optical NAND logic gate. The optical power calculations in the numerical simulation use the Poynting vector formulation of electromagnetic waves. For the z-direction propagation wave [36], the total power in x-y plane is obtained as

$$P_z = P_{z-x} + P_{z-y} \tag{6}$$

where the *x*-direction polarized component is

$$P_{z-x} = \mathrm{Re}\left(\frac{1}{2}\iint_s E_x H_y^* dxdy\right) \quad (7)$$

and the *y*-direction polarized component is

$$P_{z-y} = -\mathrm{Re}\left(\frac{1}{2}\iint_s E_y H_x^* dxdy\right) \quad (8)$$

The Poynting vector is a complex quantity, where only the amplitude levels are used to determine the logic states. In Fig. 6, the resolving electric field E_y amplitude simulation in the *y*-direction provides a certain Poynting vector pattern, and a beam propagation of equivalent output signal. Therefore, based on the output strength obtained at the port D, several parameters were used to analyze the device's performance, and made available in Tab. IV.

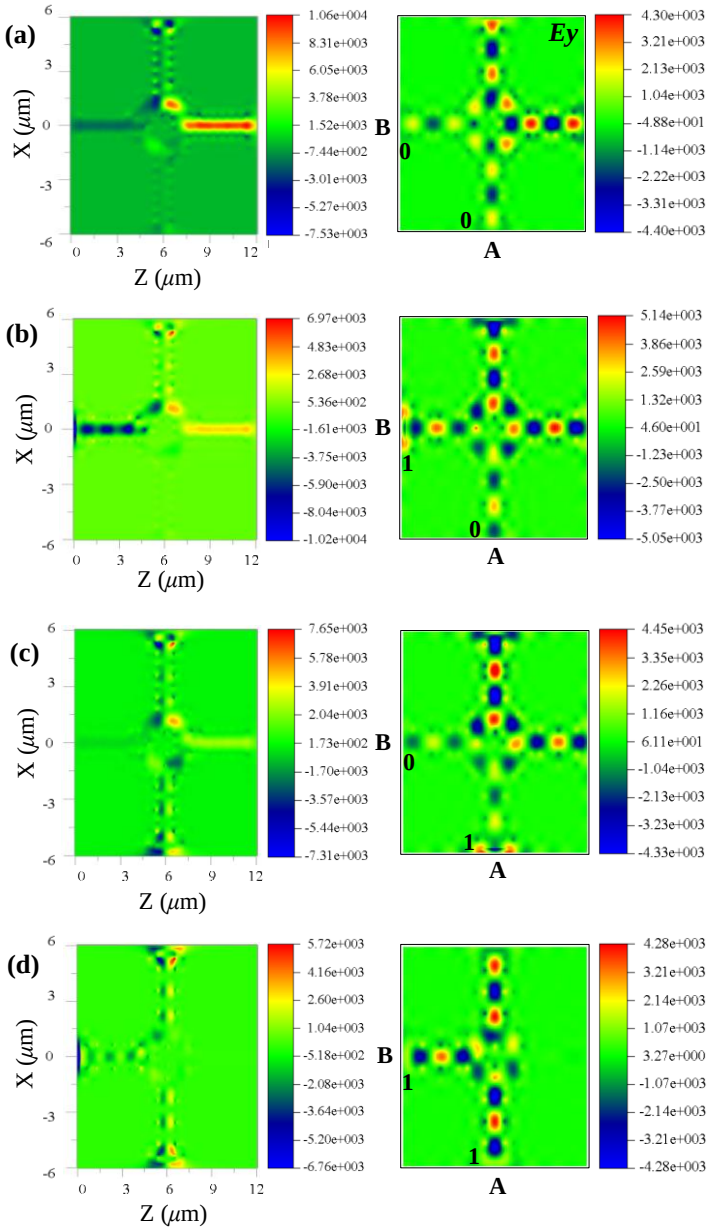

Fig. 6. The Poynting vector pattern of the NAND functionality at operational wavelength of 1700 nm and the electric field (E_y) distribution simulation in the 2D-PhC structure in cases (a) 0 – 0; (b) 0 – 1; (c) 1 – 0, and (d) 1 – 1.

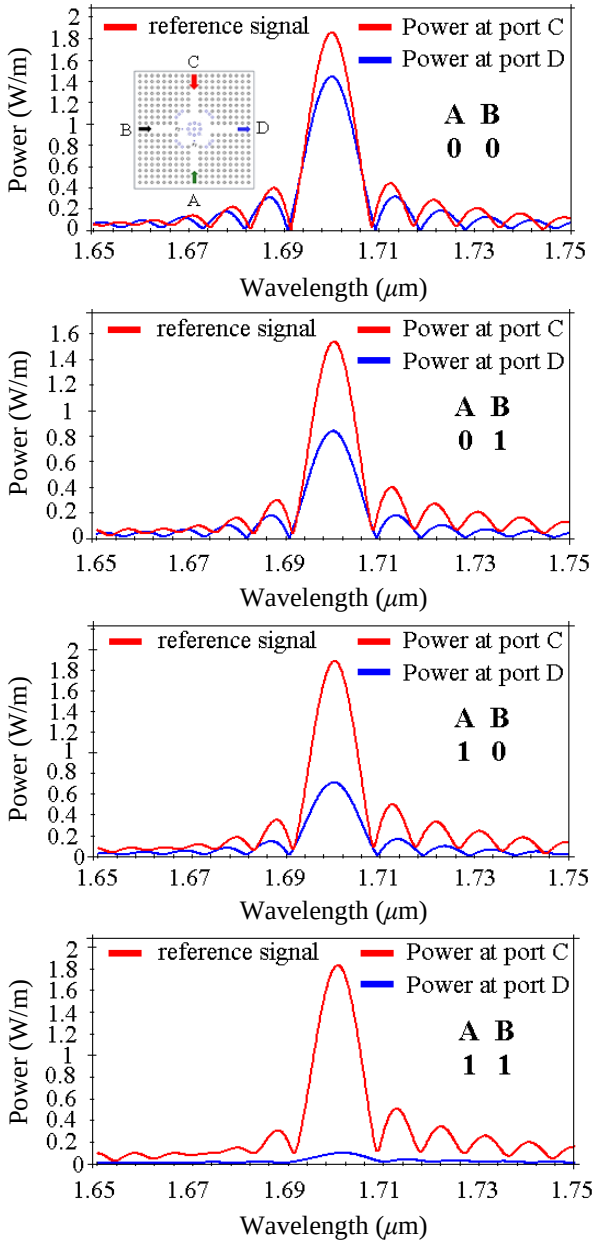

Fig. 7. The power level transmitted at the output port D when at port C is applied the pumping optical source for the different input combinations (a) 0 – 0; (b) 0 – 1; (c) 1 – 0, and (d) 1 – 1.

Fig. 6 and Fig. 7 show: case (a), when port A and port B are in OFF state (bit 0), and at the reference port C is applied the pumping optical source with a phase of 0°, so due to the rods with radius r_1 and r_2, the optical signal from the reference port C will propagate towards the output port D (bit 1). Thus, the electric field *Ey* propagation results show the switching capability. In this case, the optical source at the reference port C is responsible for obtaining the desired functionality of the logic gate.

In case (b), there is an optical signal output at port D (bit 1) due to the operation of the central PCRR, while that in reference port C the pumping optical source is applied with phase 0°. In this precise case, no input signal is applied at port A (bit 0), while an optical signal is applied at port B (bit 1) with phase of 0°. Thus, constructive interference occurs and the light pulse will propagate towards the port D.

In case (c), there is also high optical signal in port D (bit 1) when the input ports A and B invert the status. It means that no signal is applied at input port B (bit 0), whereas that at the input port A, an optical signal is applied with phase 0° (bit 1). The phase of reference beam at port C is 0°. Therefore, constructive interference occurs, and due to the rods with radius r_1 and r_2, the light pulse will propagate towards the port D.

Finally, in case (d), a minimum optical signal will propagate towards the port D (bit 0). In this case, the optical source is applied at both the input ports A and B with a phase of 180° and 0°, respectively (bit 1). The optical signal is applied at the reference port C with a phase of 0°. In this specific case, both destructive and constructive interference will takes place, respectively, and is detected a level very low of power signal at port D.

TABLE III
POSSIBLE INPUT COMBINATIONS AND REQUIRED PHASE VALUES FOR NAND FUNCTIONALITY.

Inputs		Phase angle		Output
A	B	ϕ_A	ϕ_B	
0	0	–	–	1
0	1	–	0°	1
1	0	0°	–	1
1	1	180°	0°	0

The phase of input light beam from ports A and B for NAND logical function is shown in Tab. III.

Analyzing the simulation results shows that the output port D achieves logic ‘1’ from 78 fs onwards for NAND functionality, as evident in Fig. 8.

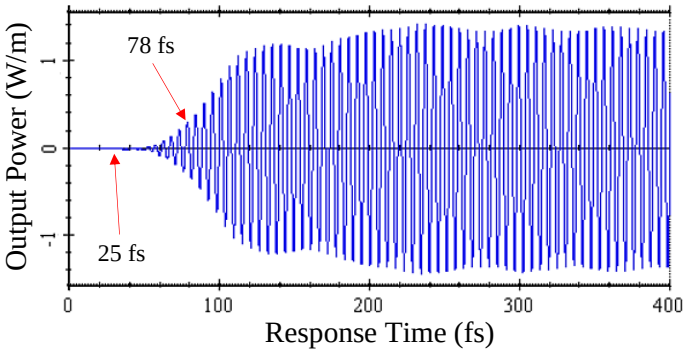

Fig. 8. Response time curve for NAND logic gate.

The maximum *CR* of the NAND port is calculated to be 12.04 dB, the minimum *CR* is 8.97 dB, and the *Q*-factor is found to be 220.5, indicating a high performance without the use of optical amplifiers.

According to the simulation results in this paper, the maximum insertion loss of structure in $\lambda = 1700$ nm is minimal, about -1.52 dB. This insertion loss is excellent for the proposed structure. The NAND logic gate has a response time and bit rate of 0.025 ps and 40 Tbps, respectively.

The Tab. IV summarizes important performance parameters of the device. The performance results of the proposed device were compared with the performance of some NAND logic gates that have been published in recent years [3, 4, 28, 36-40].

Tab. IV shows that the proposed structure in our work has a high contrast ratio, better than the other works in [3], [4], [28], [36], [40].

Furthermore, the proposed NAND logic gate has a small size compared to other structures [4], [28], [36]-[39], contributing to an increase of integration density of components miniaturized and high performance. The Tab. IV shows that our structure has a higher operational speed when compared to existing works [3], [4], [36], [38], [40].

In general, Tab. IV shows that our design presents significant advantages in parameters such as size, output power, contrast ratio, quality factor, response time, bit rate and energy consumption.

TABLE IV
A COMPARISON OF SOME NAND LOGIC GATES BASED ON 2D PHOTONIC CRYSTALS.

Ref.	Size (μm × μm)	Output (W/m)	Maximum *CR* (dB)	Insertion loss (dB)	*Q*-factor	Response time (ps)	Bit rate (Tbps)
[3] (2023)	114 μm^2	NR	10.31	NR	NR	NR	5
[4] (2020)	424.7 μm^2	1.2	5.79	NR	NR	0.25	4
[28] (2019)	12.5 × 12	NR	8.47	NR	NR	NR	NR
[36] (2020)	22.1 × 9.1	0.22	5.29	NR	NR	0.56	1.79
[37] (2020)	471.32 μm^2	NR	13.97	NR	NR	NR	NR
[38] (2021)	988 μm^2	NR	NR	NR	NR	2.5	NR
[39] (2021)	192 μm^2	0.55	NR	NR	NR	NR	NR
[40] (2023)	9 × 9	0.89	11.71	0.01	NR	0.0278	35.9
This Work	12 × 12	1.44	12.04	1.52	220.5	0.025	40

abbreviation: NR = Not Reported.

V. CONCLUSION

The proposed structure can operate as a NAND gate and exhibits a response time of approximately 25 fs. The electromagnetic simulation results using the FDTD method show that the proposed all-optical switching is a strong candidate to be used for ultrafast optical digital circuits. Furthermore, the results show that PCRR plays an essential role in the switching capacity of the NAND logic gate. Moreover, compared with conventional PhC-based all-optical logic gates, the structure of the proposed NAND gate has very small size of about 12 μm × 12 μm and can work with low power consumption, without use of the optical amplifiers and nonlinear materials. Because of their small size, this device is suitable for usage in PICs, in ultrafast applications.

Finally, the performance parameters show that the simulated structure is promising for applications in optical communications systems, optical integration circuits, on ultrafast all-optical operations in digital processing systems, computing, among others.

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