An Analog Filter Bank-based Circuit for Performing the Adaptive Impedance Matching in PLC Systems

Luis Guilherme da S. Costa, Antônio Carlos M. de Queiroz, Vinicius L. R. da Costa, and Moisés V. Ribeiro

***Abstract*—Aiming to bring attention to the necessity of dealing with the dynamics of access impedance in electric power systems, this paper introduces an adaptive impedance matching circuit that is based on an analog filter bank approach. In this sense, it describes a prototype that validates the proposed filter bank approach for improving impedance matching. Numerical results obtained with the detailed prototype operating in the frequency band between 2 and 500 MHz show that the proposed analog filter bank approach helps to improve impedance matching in power line communication (PLC) systems. Also, the numerical results show that the dynamics of impedance matching between two or more PLC transceivers is a difficult task to be accomplished because real-time coordination among them is necessary. Overall, it is shown that the proposed analog filter bank approach constitutes an interesting research direction for improving impedance matching between PLC transceivers and electric power systems.**

***Index Terms*—power line communication, coupling, impedance matching, analog filter, electric power system.**

I. Introduction

In the past few decades, power line communication (PLC) systems have proven themselves as an additional and effective data communication technologies since they allow the use of electric power system infrastructures as a means for data communication purposes [1]–[5]. However, the dynamics of loads; electromagnetic interference associated with the use of unshielded power cables; significant signal attenuation with the distance and frequency increase; channel frequency selectivity due to multi-path signal propagation; high power impulsive noises yielded by switching devices; and impedance mismatching between branching points and the points of connection turn electric power systems hard data communication media [1].

Concerning the impedance mismatching problem as a typical data communication system, the transmitter output and receiver input impedance must be designed to ensure impedance matching with a constant-value line impedance and, consequently, maximize the power transfer. However, PLC systems face a challenging scenario because the access impedance of electric power systems changes in the time and frequency domains due to the dynamics of loads [6]. Regarding only the frequency domain, literature has shown that access impedance exhibits frequency selectivity for the frequency bandwidths occupied by narrowband and broadband PLC systems, constituting a rather tricky scenario to achieve impedance matching [6]–[8] effectively. However, the effective design of impedance matching circuit between PLC transceivers and electric power systems plays a vital role in maintaining the appropriate signal strength at the point of connection with electric power systems. In other words, it has to be accomplished to assuring the maximum power transfer that positively impacts reliability or data rate of PLC systems [9]. The dynamics of the access impedance of electric power systems at the point of connections have consistently been recognized as one of the significant weaknesses of PLC systems [10].

Few contributions address impedance mismatching between PLC transceivers and electric power systems [11]–[13] since loads mainly control the dynamics of impedance access in electric power systems, and these loads can hardly be controlled. Therefore, typical PLC coupling circuits present an optimum performance only at the frequency at which the impedance of electric power systems and the PLC coupling circuits match. Variations on the topology of electric power systems combined with an unknown power cable and load access impedance changes constantly the impedance matching of PLC coupling circuits based on the use of constant input/output impedance. Recent research findings suggest a manual adaptation of the access impedance of PLC transceiver to ensure its value is roughly equal, on average, to a chosen electric power systems impedance by changing the turns winding ratio $1 : N$ of a Radio Frequency (RF) transform [14], [15]. In [16], the authors proposed two different PLC coupling circuits, incorporating a $4 : 1$ and $2 : 1$ winding ratio for permanent connection between PLC transceivers and electric power systems for impedance matching purpose. As reported in [17], typical residential rooms are classified to propose proper coupler winding ratios for impedance adaptation. Couplers with specific access impedance values can result in substantial transmission gains. Regardless of the topology of electric power systems, gains up to 10 dB can be attained [17].

Regarding the adaptive PLC coupling circuits for impedance matching, it is well-established that the previous investigations have not introduced solutions for all scenarios. For instance, [9], [18] considering flaws of size, cost, and performance while [19] discussing in a coupling circuit, which is dynamically adapted by tuning its inductors and the RF transform of the PLC coupling circuit with a fuzzy logic technique

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implemented in a microcontroller. Also, [20] discussed a voltage controllable inductance circuit, which is composed of an operational amplifier, for performing impedance matching through the use of a voltage controllable inductance circuit. In [21], the authors emphasized the benefits of active inductors over a tapped transformer and the use of a digital variable capacitor controlled by a microcontroller. Transformerless impedance matching circuits combined with capacitor banks and active inductor topologies were proposed in [22]. In [23] was introduced an adaptive impedance matching circuit that automatically tries to match impedance, changing the tap of the RF transformer, which is controlled by a microcontroller that makes use of a feedback circuit for measuring the reflected power of the signal injected by PLC transceivers into electric power systems.

A critical aspect of impedance matching is the frequency bandwidth. The Smith Chart gives a good match at a single frequency, but a broadband design is often required. The Bode-Fano criterion [24] relates the quality of the matching to the frequency bandwidth. This criterion shows that a perfect match is only possible if we assume very narrow frequency bandwidth or a single frequency. Broadband impedance matching with cascaded L-Networks is accomplished by cascading more sections of filters with additional intermediate impedance, creating lower impedance rates and correspondingly lower Q-factor for each filtering section. However, it depends on the loads and electric power systems impedance, which vary in time and frequency. Consequently, a PLC coupling circuit needs an adaptation in the cascade L-Networks every time access impedance of electric power systems impedance change to ensure maximum power transfer [12]. The effectiveness of the impedance matching based on L-Networks depends on the insertion loss level.

Aiming to improve the impedance matching between PLC transceivers and electric power systems, this paper introduces the use of an analog filter bank approach to come up with feasible adaptive PLC coupling circuits. In this sense, the filter bank-based impedance matching circuit measures the received signal's power and compares it with a typical value memorized in a control unit. It switches between different impedance matching circuits (analog and low-pass filters), which are supposed not to reflect signals in their band-pass to the source, for performing impedance matching in the chosen frequency band. The main contributions of this study are summarized as follow:

- The formulation of impedance mismatching for PLC systems as a problem that is time-varying and frequency selective, and, as a consequence, the discussion about the necessity of adapting the access impedance of PLC transceivers to deal with the dynamics of electric power systems is well-posed.
- The discussion on the *principle of divide and conquer*, the coherence bandwidth, and the coherence time to introduce a filter bank approach for performing adaptive impedance matching. Based on this approach and assuming that the number of analog filters in the filter bank is correctly designed, the impedance matching can theoretically be accomplished.
- A detailed description of the prototype of an adaptive, broadband, capacitive, Single Input Single Output (SISO), and low-voltage (LV) PLC coupling circuit for validating the proposed approach. The prototype implements a filter bank-based impedance matching circuit that is controlled by a microcontroller. This prototype covers the frequency bands of $2-50$ MHz, $2-100$ MHz, and $2-500$ MHz. Also, discussions about the performance of the prototype in three setup arrangements are outlined.

Based on the numerical results, the following statements deserve attention:

- The analog filter bank approach is an appealing research direction when frequency bandwidth is broad, and the access impedance of electric power systems is time-varying and frequency selective. Also, it was shown that the coherence bandwidth of the magnitude of the access impedance is the correct parameter to guide impedance matching because the impedance is almost constant in a frequency bandwidth shorter than the coherence bandwidth. Moreover, if it is performed in a time interval shorter than the coherence time of the access impedance of electric power systems, then the time-varying behavior can be handle in an elegant manner. Under this constraint, the adaptive coupling circuits can be designed for accomplishing impedance matching purposes.
- The implemented prototype shows that the access impedance of PLC transceivers adapts by switching among the circuits belonging to the analog filter bank, which results in feasible adaptive PLC coupling circuits if the complexity of the analog filter bank (i.e., the number of analog filter) is small. Numerical results show that the best impedance matching is achieved for the PLC coupling circuits with an input impedance of $50\ \Omega$ and $100\ \Omega$ while the PLC coupling circuits with an input impedance of $25\ \Omega$ offered the worst results in terms of $S_{11}(f)$ and $S_{12}(f)$ scattering parameters.
- The setup arrangements for characterizing $S_{11}(f)$ and $S_{21}(f)$ scattering parameters show important information concerning attenuation and reactive behaviors of electric power systems, mainly in the presence of the adaptive PLC coupling circuit operating in the frequency band of $2-500$ MHz. Also, numerical results of $S_{11}(f)$ scattering parameter show that it may be challenging to perform impedance matching between two or more adaptive coupling PLC circuits because real-time coordination among them may be necessary.

The remainder of this paper is organized as follows: Section II formulates the impedance mismatching problem related to PLC systems; Section III discusses the analog filter bank approach for performing impedance matching by PLC transceivers; Section IV outlines the implementation of the adaptive, broadband, capacitive, SISO and LV PLC coupling circuit based on the analog filter bank approach; experimental results are presented in Section V while concluding remarks are stated in Section VI.

II. Problem Formulation

Several practical questions arise concerning the impedance mismatching in narrowband and broadband PLC coupling circuits. For instance, electric power systems differ considerably in terms of topologies, connected loads, physical characteristics of the electromagnetically unshielded power cables, types of soils, and the distances from the soil and between power lines.

Considering electric power systems be time-varying systems, we can use the two-wire transmission line theory to adapt two-port $ABCD$ matrices to model the signal propagation and analyze impedance mismatching [25], [26] in a time-varying scenario. Fig. 1 shows a model based on the $ABCD$ matrix that can be used to analyze the impedance mismatching problem related to PLC systems. This model emphasizes that PLC transceivers and electric power systems are time-varying systems. Noting that electric power systems time-varying behavior is mainly associated with load dynamics owned by electric utilities and consumers. Also, since the coherence time of in-home and LV is lower than 600 μs [27], [28] and around 1000 μs for outdoor and LV electric power systems, we can assume during these time intervals that electric power systems are time-invariant systems, and consequently they can be modeled by a well-known $ABCD$ matrix. In other words, during the time interval $t \in [0, T_c]$, in which T_c denotes the coherence time of the PLC channel, the $ABCD$ matrix presents irrelevant changes, and T_c can be seen as a great approximation of the coherence time for the access impedance of electric power systems.

According to Fig. 1, we have

$$\begin{bmatrix} V_1(f,t) \\ I_1(f,t) \end{bmatrix} = \begin{bmatrix} A(f,t) & B(f,t) \\ C(f,t) & D(f,t) \end{bmatrix} \begin{bmatrix} V_2(f,t) \\ I_2(f,t) \end{bmatrix}, \quad (1)$$

in which $V_{TX}(f,t)$ is the voltage source with $Z_{TX}(f,t)$ internal impedance; $V_1(f,t)$ and $I_1(f,t)$ are, respectively, the voltage and current at the input port of the electric power circuit; $V_2(f,t)$ and $I_2(f,t)$ are the voltage and current at the output port of the electric power circuit, respectively; $V_{RX}(f,t) = V_2(f,t)$ is the voltage at the input port of the PLC transceiver; $Z_{RX}(f,t)$ is the impedance at the input port of the PLC transceiver; and $Z_1(f,t)$ and $Z_2(f,t)$ are the access impedance at the input and output port of the electric power circuit, respectively. Note that $V_1(f,t) = V_{TX}(f,t) - Z_{TX}(f,t)I_1(f,t)$ which is the voltage at the input port of the two-port $ABCD$ of the electric power circuit. The voltage $V_{RX}(f,t)$ at the receiver of the PLC transceiver, which has an impedance $Z_{RX}(f,t)$, is given by

$$V_{RX}(f,t) = V_2(f,t) = Z_{RX}(f,t)I_2(f,t). \quad (2)$$

The relations between the input and output ports of the two-wire transmission line showed in Fig. 1 can be obtained using

$$\begin{aligned} V_1(f,t) &= A(f,t)\,V_2(f,t) + B(f,t)\,I_2(f,t) \\ I_1(f,t) &= C(f,t)\,V_2(f,t) + D(f,t)\,I_2(f,t). \end{aligned} \quad (3)$$

Note that the two-port network can be written as a function of the input impedance parameters, $Z_1(f,t)$, of an electric power circuit. It can be obtained by time-varying $ABCD$ matrix, see (1). As a result,

$$Z_1(f,t) = \frac{V_1(f,t)}{I_1(f,t)} = \frac{A(f,t)\,Z_{RX}(f,t) + B(f,t)}{C(f,t)\,Z_{RX}(f,t) + D(f,t)}. \quad (4)$$

It means that the input access impedance parameter of the electric power circuit depends on the time-varying behavior of input impedance $Z_{RX}(f,t)$ of the PLC transceiver and $ABCD$ matrix of the electric power circuit [29]. Thus, we can conclude that to maximize the power transfer from the transmitter to the receiver, the PLC coupling circuit must be designed to precisely match the time-varying behavior of the impedance of input and output ports of an electric power circuit. Also, such circuit is modeled as a time-varying $ABCD$ matrix, with the $Z_{TX}(f,t)$ and $Z_{RX}(f,t)$ impedance of the PLC transmitter and receiver, respectively.

The use of concepts of impedance matching and $ABCD$ matrix can help to understand the impedance mismatching between PLC transceivers and electric power systems when the dynamics of loads are taken into account. For instance, in Fig. 1, $Z_1(f,t)$ represents the impedance of the electric power system seen by the transmitter of the PLC transceiver, which could be matched with the impedance $Z_{TX}(f,t)$. On the other hand, $Z_2(f,t)$ is the electric power systems impedance seen by the $Z_{RX}(f,t)$ impedance of the PLC transceiver. Note that $Z_{TX}(f,t) = Z_1(f,t)$ and $Z_{RX}(f,t) = Z_2(f,t)$ means that maximum power transfer occurs between PLC transmitter and electric power systems and between electric power systems and PLC receiver, respectively.

At this moment, it is important to emphasize that the access impedance of electric power systems is continuously changing as time evolves. Consequently, it is challenging to achieve perfect impedance matching if $Z_{RX}(f,t)$ and $Z_{TX}(f,t)$ are not designed by taking into account the time variable, t, (i.e., the time-varying behavior of electric power systems).

Based on this scenario, it is clear that the impedance matching between PLC transceivers and electric power systems demand the design of the adaptive PLC coupling circuits that are capable of detecting variations of access impedance of electric power systems and dynamically adjust the impedance of the coupling circuit. Section III outlines an approach to deal with this problem.

III. Analog Filter Bank Approach for Impedance Matching

Let $Z(f,t)$ be the access impedance of an electric power system, such as $-\infty < t < +\infty$, $B \in \mathbb{R}_+ | \, |f| \leqslant B$ is the frequency bandwidth in Hertz. Then, the following definitions apply:

Definition 1. *The coherence time of $Z(f,t)$ is denoted by $T_z \in \mathbb{R}_+$. The coherence time of the access impedance refers to a time interval duration in which $Z(f,t) \approx Z(f,t+\Delta t)$ subjected to $\Delta t \in \mathbb{R}_+ | \, \Delta t \leqslant T_z$. The coherence time is defined by*

$$\begin{aligned} T_z &\triangleq \texttt{arg max}\, R_T(\Delta t) \\ &\texttt{subject to}\ |R_T(\Delta t)| \geqslant \alpha, \end{aligned}$$

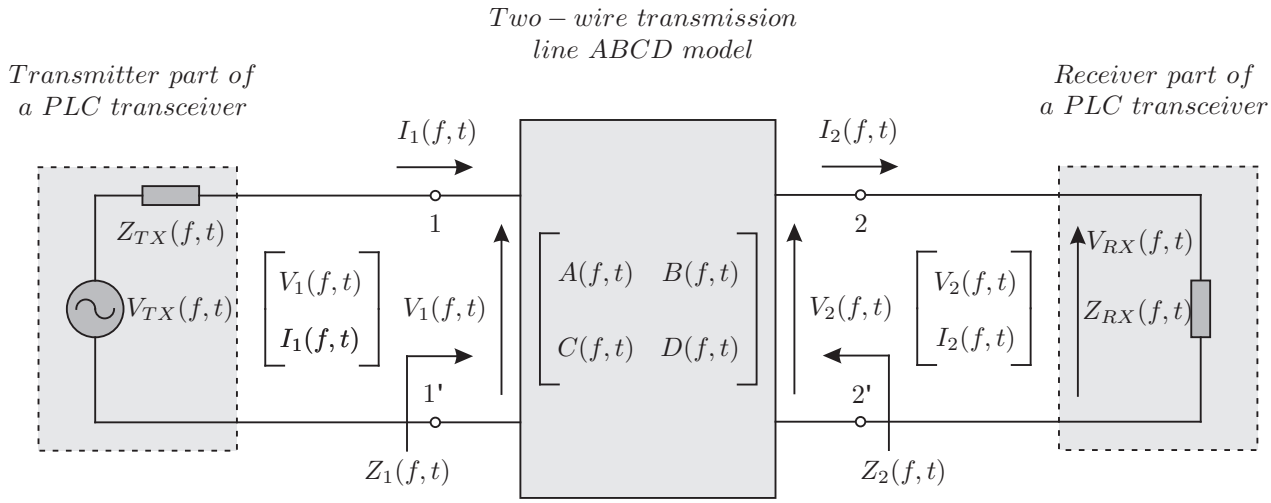

Fig. 1: Two-port $ABCD$ time varying matrix model for dealing with the dynamic of electric power systems.

in which

$$R_T(\Delta t) = \frac{\left|\iint Z(f,t)Z^*(f,t+\Delta t)dfdt\right|}{\iint |Z(f,t)|^2 dfdt}, \tag{5}$$

$\alpha \in \mathbb{R}_+ | \ 0 < \alpha < 1$, $|\ |$ *is the absolute value operator and* $*$ *is the complex conjugate operator.*

Definition 2. *The coherence bandwidth of* $Z(f,t)$ *is denoted by* $B_z \in \mathbb{R}_+$*. The coherence bandwidth refers to a frequency bandwidth in which* $Z(f,t) \approx Z(f+\Delta f,t)$ *subjected to* $\Delta f \in \mathbb{R}_+ | \ \Delta f \leqslant B_z$*. The coherence bandwidth is defined by*

$$B_z \triangleq \texttt{arg max}\, R_B(\Delta f)$$
$$\texttt{subject to}\ |R_B(\Delta f)| \geqslant \beta,$$

in which

$$R_B(\Delta f) = \frac{\left|\iint Z(f,t)Z^*(f+\Delta f,t)dfdt\right|}{\iint |Z(f,t)|^2 dfdt} \tag{6}$$

and $\beta \in \mathbb{R}_+ | \ 0 < \beta < 1$.

Based on the aforementioned definitions, the following theorems apply:

Theorem 1. *Let the access impedance of an electric power system be given by* $Z(f,t) \in \mathbb{C}$*, then* $Z(f+\Delta f, t+\Delta t) = Z$ *for* $\Delta f \in \mathbb{R}_+ | 0 \leqslant \Delta f \leqslant B_z$ *and* $\Delta t \in \mathbb{R}_+ | 0 \leqslant \Delta t \leqslant T_z$*.*

Proof. According to [28], [30], the data communication channel between two PLC transceivers become time-invariant during a period shorter than the so-called coherence time of PLC channel, T_c. In addition, [31]–[33] states that the frequency response of any quantity can be constant in a frequency bandwidth shorter than the so-called coherence bandwidth. Assuming that $T_z \approx T_c$, which is an acceptable assumption due to the intrinsic relationship among the scattering parameters and the value of the coherence bandwidth of the access impedance of electric power systems, it is easy to conclude that $Z(f+\Delta f, t+\Delta t) = Z$ for $0 \leqslant \Delta f \leqslant B_z$ and $0 \leqslant \Delta t \leqslant T_z$. □

Lemma 1. *In the* n^{th} *time interval denoted by* $T_{z_n} \in [nT_z \leqslant t \leqslant (n+1)T_z]$*, the value of the access impedance in the* k^{th} *frequency sub-band, which occupies* $(2k-1)B_z/2 \leqslant f \leqslant (2k+1)B_z/2$*, is a constant value denoted by* $Z_{k,n} \in \mathbb{C}$*.*

Proof. Let us assume that T_c is long enough for processing $Z(f,t)$ during the n^{th} time interval, then the impedance matching between PLC transceivers and electric power systems, in the whole frequency band, can be accomplished by using *the principle of divide and conquer*. The use of this principle in the impedance mismatching problem results in the decomposition of the broadband impedance mismatching problem into $J \in \mathbb{N} | J \triangleq \lceil B/B_z \rceil$, where $\lceil x \rceil = \min l \in \mathbb{N} \,|\, l > x$, narrowband and parallel impedance mismatching problems. Constant impedance values characterize these problems because the Theorem 1 states that during the n^{th} time interval, the access impedance of electric power systems can be approximated by a piece-wise constant function within the frequency band shorter than B_z. Consequently, impedance matching can be easily designed for each constant piece of the frequency response of the access impedance, which is supposed to be time-invariant in a time interval shorter than T_z. □

The implementation of the Lemma 1 for performing impedance matching between PLC transceivers and electric power systems can be accomplished by using a bank of J impedance matching sub-circuits with each of them designed to match a constant impedance in a bandwidth equal to B_z. In this sense, the block diagram of the so-called impedance matching circuits bank for a PLC transceiver is shown in Fig. 2. According to this block diagram, the bank of impedance matching circuits can be divided into four main parts: the interface with electric power systems, two switching banks, the impedance matching circuits bank, and the control unit. Note that J sub-circuits constitute the m^{th} impedance matching circuit for performing impedance matching in the J sub-bands of frequency bandwidth equal to B_z, which is a consequence of using the *principle of divide to conquer*. Based on the summation of the signal available at the outputs of the Switch

Bank #2, the Control Unit applies a control algorithm to simultaneously control the Switch Banks #1 and #2 to select the best impedance matching and to ensure that the impedance matching is accomplished in a time interval shorter than T_z. It is important to emphasize that as long as $T_z \to \infty$, the switching process facilitates because electric power systems tend to be time-invariant ones.

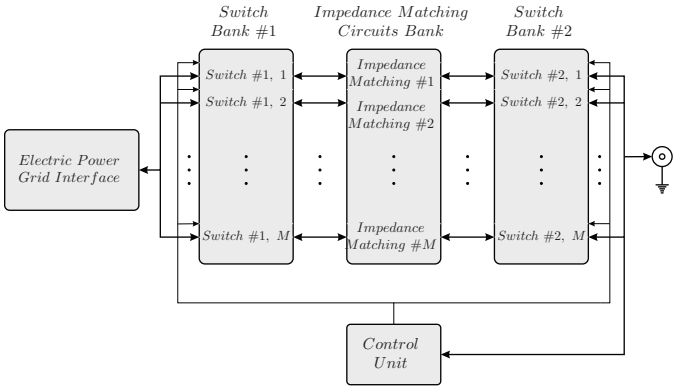

Fig. 2: The block diagram of impedance matching circuits bank for a PLC transceiver.

Note that the Control Unit samples the signal available at the Switch Bank's outputs #2 and calculates average power values for all M impedance matching circuits. The average power values in the discrete-time domain are given by

$$P_{v_{\text{avg}}}[m] = \big(1/N\big) \sum_{i=1}^{N} v^2[m,i], \tag{7}$$

where $1 \leq m \leq M$, $N \in \mathbb{N}$ is the number of samples, $v[m,i]$ is the i^{th} sampled value from the j^{th} output of the Switch Bank #2. The j^{th} impedance matching circuit offering the highest average power is chosen to perform impedance matching. Note that other values, such as the average signal value, can be applied to reduce computational complexity.

Using the Control Unit and the Switch Banks #1 and #2, the impedance matching can be accomplished through two different strategies, which are described as follows:

- Strategy #1: Each impedance matching sub-circuit is designed to match the access impedance associated with one frequency sub-band, which occupies a frequency bandwidth equal to B_z. This strategy may result in the best impedance matching results. Indeed, if $B_z \to 0$ (i.e., $J \to +\infty$), then the impedance matching circuits bank tends to correctly perform the impedance matching between PLC transceivers and electric power systems with a large number of matching circuit in parallel and, as a consequence, it may show it may result in an unfeasible and costly solution because of the considerable hardware complexity. Therefore, a careful choice of J and M may result in a reasonable trade-off between performance and complexity.
- Strategy #2: All impedance matching sub-circuits are designed to match the access impedance associated with the whole frequency band (i.e., $B_z = B$), which imposes $J = 1$. If the frequency bandwidth of the access impedance, B, is small, and consequently, the corresponding magnitude of the frequency response is flat, then the impedance matching can be easily accomplished with well-known techniques. This strategy can offer an impedance matching performance that depends upon the frequency selectivity of the access impedance in the whole frequency band. Moreover, it results in a feasible and not expensive solution because the hardware complexity is reasonable if a careful choice of M applies.

It is important to emphasize that the impedance matching circuits bank can be feasible and reasonably effective if the following issues are correctly addressed:

- The number of impedance matching circuits JM must be carefully chosen because it dictates the hardware complexity. For practical reasons, J and M must be small (e.g., $J \leq 5$ and $M \leq 5$).
- The correct specification of switches because their transients can remarkably influence the overall performance.
- The choice of reflectionless analog filters are advantageous because they do not reflect signals in their stopbands back to the source. Also, the analog filters must be capable of matching with a pre-specified set of impedance values covering the frequency bandwidth equal to B_z.
- The choice of impedance matching circuits has to match the access impedance of electric power systems in some sense; otherwise, it will not be effective.

IV. Validation through a prototype: The implementation of Strategy #2

The main objective of a PLC coupling circuit is to perform impedance matching and filter the undesirable signals with simple, effective, and low-cost electronics. In this regard, this section addresses the implementation of Strategy #2, in which the analog filter banks are responsible for implementing the impedance matching circuits. Each impedance matching circuit is designed to offer a reasonable trade-off between performance and complexity, leading to good power transfer between PLC transceivers and electric power systems.

Based on the Strategy #2, Fig. 3 shows the schematic of an adaptive, broadband, capacitive and SISO PLC coupling circuit for LV electric power systems operating in frequency bands of $1.7-50$ MHz, $1.7-100$ MHz, and $1.7-500$ MHz, in which $J = 1$ and $M = 3$. We can see that it is constituted by interface and protection circuits to connect it to an electric power system, an analog filter bank, and switching for performing impedance matching, a microcontroller, and a logarithmic amplifier for implementing the Control Unit. Note that $J = 1$ and $M = 3$ result in a low complex hardware implementation.

The top and bottom (layers view) of the two-layer fiberglass printed circuit board (PCB) of this adaptive PLC coupling circuit, that was designed in Altium software, are shown in Figs. 4 and 5, respectively. The PCB was designed following the microstrip technique [34], and only Surface Mounted Device (SMD) components were used because their usage reduces the PCB area and covers the chosen frequency bands. Tab. I lists the components used for implementing this adaptive PLC coupling circuits. Details about the main parts of the

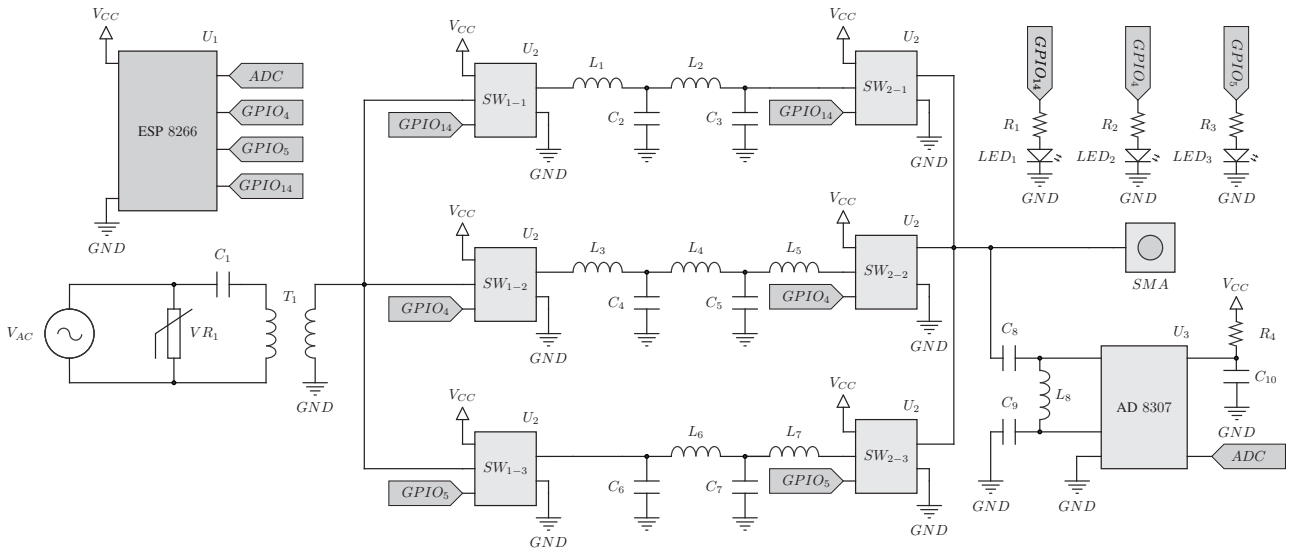

Fig. 3: The schematic of the adaptive, broadband, capacitive, SISO and LV PLC coupling circuit with $J = 1$ and $M = 3$.

adaptive, broadband, capacitive, SISO and LV PLC coupling circuit are given in the following subsections.

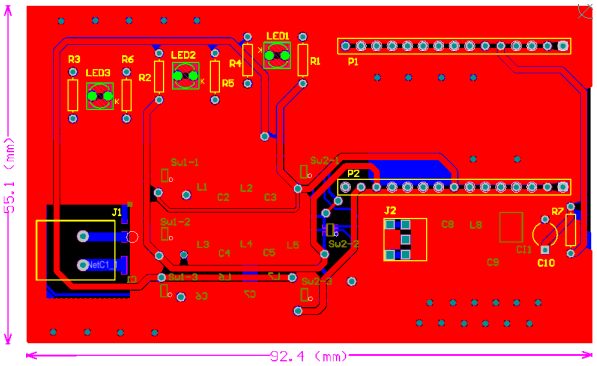

Fig. 4: The top layer of the PCB of the adaptive, broadband, capacitive, SISO and LV PLC coupling circuit.

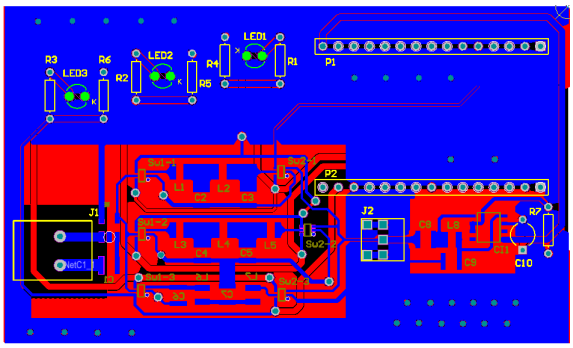

Fig. 5: The bottom layer of the PCB of the adaptive, broadband, capacitive, SISO and LV PLC coupling circuit.

TABLE I: Detail of the components used in the prototype of the adaptive PLC coupling circuit.

Component	$1.7-50$ MHz	$1.7-100$ MHz	$1.7-500$ MHz
T_1	TC1-1TX+	TC1-1TX+	TC1-1TX+
C_{BLOCK}	1.5 nF	1.5 nF	1.5 nF
L_1	100 nH	56 nH	10 nH
L_2	220 nH	120 nH	22 nH
L_3	270 nH	120 nH	27 nH
L_4	390 nH	180 nH	39 nH
L_5	270 nH	120 nH	27 nH
L_6	470 nH	220 nH	39 nH
L_7	220 nH	100 nH	18 nH
L_8	1500 nH	680 nH	82 nH
C_2	180 pF	82 pF	18 pF
C_3	82 pF	39 pF	8.2 pF
C_4	82 pF	39 pF	6.8 pF
C_5	82 pF	39 pF	6.8 pF
C_6	39 pF	22 pF	3.9 pF
C_7	82 pF	47 pF	10 pF
C_8	47 pF	33 pF	4.7 pF
C_9	33 pF	27 pF	6.2 pF
R_1-R_4	470 Ω	470 Ω	470 Ω

A. *Electric power systems interface*

Fig. 3, Fig. 4 and Fig. 5, show that the connection with an electric power system is through a KRE connector labeled J_1. The connector J_1 is followed by a protection circuit composed of a varistor VR_1 and a capacitor C_1. The varistor aims to protect the circuit against voltage transients while the capacitor blocks the mains voltage. The RF transformer named TC1-1TX+ (T_1), which operates in the frequency band of $0.4-500$ MHz [35], is chosen to achieve galvanic isolation and to offer the desired voltage ratio.

B. *Switch Banks*

The primary purpose of the RF Switch Banks is to route signals through the analog filters with the lowest insertion loss, the highest return loss, and the highest isolation between the

interface with the electric power system and the output of the impedance matching circuits bank (i.e., the analog filter bank). The control unit controls the switches operational state. Only two switches are selected in an operational state, and only one analog filter of the impedance matching circuits bank is used, while the other $M-1$ switches present a high impedance in their ports.

In Fig. 3, the components SW_{1-1}, SW_{1-2}, SW_{1-3}, SW_{2-1}, SW_{2-2} and SW_{2-3} refer to the switch devices. In this prototype, the switch PE 4239 [36] is chosen because it covers the frequency band from DC up to 3.0 GHz. This switch is a single-pole and double-throw (SPDT) - 1 : 2, which routes signals from one input to two output paths with an insertion loss of 0.7 dB at 1 GHz. This switch integrates on-board CMOS control logic with a low-voltage CMOS-compatible control interface controlled with either single-pin or complementary control inputs. Fig. 6 shows the block diagram of the switch PE 4239 in which the pins RF_1 and RF_2 are the output pins while the pin RF_C is the input of the signal. The signal is switched to the pin RF_1 or RF_2 based on the voltage level applied to the $CTRL$ pin.

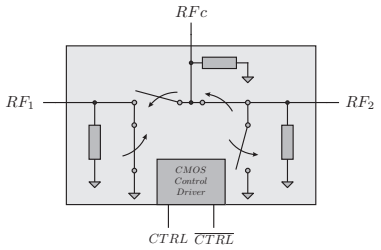

Fig. 6: The block diagram of the RF Switch PE 4239.

C. Impedance matching circuits bank

This subsection details the impedance matching circuits bank (i.e., analog filter bank), which is used in the prototype. In this regard, it is necessary to know the values of access impedance values of electric power systems. According to [31], 90% of the input resistance values measured are between 25 Ω and 100 Ω and the mean value equal to 50 Ω. Therefore, three analog filters ($M = 3$) are designed with the input resistance equal to 25 Ω, 50 Ω, and 100 Ω. The analog filters are low-pass because the signal is transmitted in the baseband. These three analog filters are designed considering input and output impedance ratios of 1 : 2 (25 to 50 Ω), 1 : 1 (50 to 50 Ω), and 2 : 1 (100 to 50 Ω), where 50 Ω is the input impedance of the PLC transceiver. Also, first (25 to 50 Ω) and third (100 to 50 Ω) analog filters are low-pass irregular ones while the second analog filter (50 to 50 Ω) is a low-pass Chebyshev one. Note that the analog filters output impedance must be matched to 50 Ω for ensuring 1 : 2, 1 : 1, and 2 : 1 ratios. Also, the input and output impedance ratios must be effective in the frequency bandwidths of the PLC coupling circuit, which are $2-50$ MHz, $2-100$ MHz, and $2-500$ MHz.

Tab. II lists the the specifications applied to design the low-pass irregular analog filters and low-pass Chebyshev analog filter with Z_{in} equal to 25 Ω, 50 Ω and 100 Ω, and cut-off frequency, f_c, of 50 MHz, 100 MHz, and 500 MHz. It is important to emphasize that the design of analog filters to perform broadband impedance matching is a very complicated task to be accomplished, and excellent results can be attained by using more complex circuits. However, we will focus on cost-effective analog filters that show the analog filter bank approach as a great potential for impedance matching purposes. See numerical results in Section V. Details about these analog filters, which are designed to perform impedance matching with the termination of unequal impedance at the input and output ports, and their design are presented in the following subsections.

TABLE II: Specification of analog and low-pass filters.

Description	Value
Input impedance Z_{in}	Z_{in} (Ω)
Output impedance Z_{out}	50 Ω
Type of analog filter	Low-pass irregular analog filter or low-pass Chebyshev analog filter
Pass-band ripple	0.5 dB
Stop-band attenuation	40 dB
Cut-off frequency	f_c (MHz)
Maximum insertion loss	-15 dB

1) Low-pass irregular analog filter: This subsection details the use of an approximation function for broadband impedance matching, which results in low-pass irregular analog filters of even order. These types of analog filters are useful to perform impedance matching when the frequency band is broad. Fig. 7 illustrates the frequency response of a low-pass irregular analog filter $|H(f)|$. Note that $|H(f_x)| = 1/\sqrt{2}$ corresponds to the 3 dB cut-off frequency, $1/\sqrt{1+\varepsilon^2}$ is the ripple of magnitude response, f_x' and f_x are the band-pass limits. This graph assumes a normalization process in which $f_x = 1$ Hz. Note that the normalization process is applied to perform the filter design.

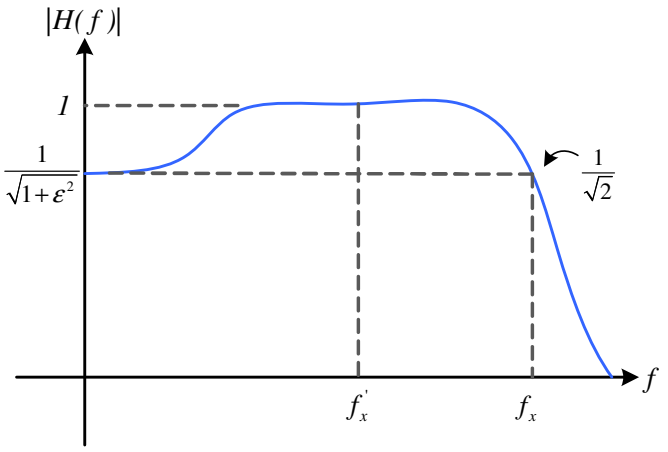

Fig. 7: Normalized frequency response of the low-pass irregular analog filter.

The magnitude of the low-pass irregular analog filter is given by [37]

$$|H(f)| = \frac{1}{\sqrt{1+|K(f)|^2}}, \tag{8}$$

where the characteristic function $K(f)$ is obtained from the Feldtkeller's equation. The band-pass, which is defined between f'_x and f_x, and the stop-band, which cover $f > f_x$, specifications must be satisfied by characteristic function $K(f)$. Notice that $K(f)$ is defined to ensure that $|K(f)|^2$ approximates to zero in the stop-band with a band-pass attenuation error or band-pass ripple given by $\varepsilon \in \mathbb{R}$ with $K(f) = F(f)/P(f)$ being an even rational polynomial function ratio, $F(f)$ the reflection zero polynomial, and $P(f)$ is the transmission zero polynomial [37]. The characteristic function between f'_x and f_x is given by

$$K\left(f\right) = \frac{F\left(f\right)}{P\left(f\right)} = \varepsilon\left(f^2 - 1\right)^2, \tag{9}$$

where $\varepsilon \in \mathbb{R}^*_+$ is a constant which is calculated in function of the source impedance $Z_S\left(f\right) = Z_S \in \mathbb{R}^*_+$ and the output impedance $Z_L\left(f\right) = Z_L \in \mathbb{R}^*_+$ impedance terminations, as shown in Fig. 8.

As stated in Section II, the impedance matching between PLC transceivers and electric power systems must cover the entire frequency band. Also, the low-pass irregular analog filters, showed Fig. 8, must be designed with low order and low-quality factor "Q" to cover the entire band of frequency. Aiming to develop low-cost implementation, we decide in favor of a 4^{th} order low-pass irregular analog filters. It is essential to mention that the low-pass irregular analog filter designed with the structure composed of the components L_1, L_2, C_2, and C_3 must be selected if the output impedance Z_L is bigger than electric power system impedance Z_S. Nonetheless, if the electric power system impedance Z_S is bigger than the output impedance Z_L, the designed low-pass irregular analog filter is constituted by the components C_6, C_7, L_6, and L_7 must be selected. P_{in} is the power delivered by the input port of the low-pass irregular analog filter, and P_{out} is the power delivered to output impedance Z_L.

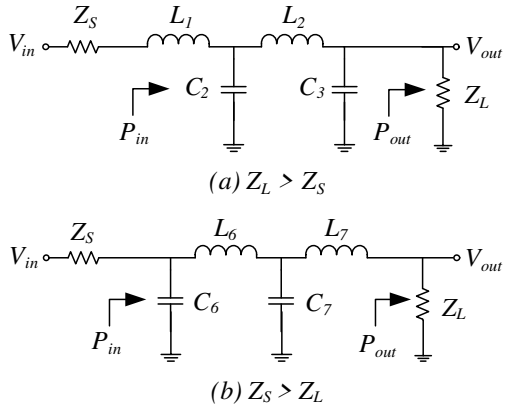

Fig. 8: The electric circuits of the designed low-pass irregular analog filters for the adaptive PLC coupling circuit.

The transduction or attenuation function $T(f) = E(f)/P(f)$ corresponding to this characteristic function is obtained by solving the *Feldtkeller's* equation, which is given by

$$E(f)E(-f) = P(f)P(-f) + F(f)F(-f). \tag{10}$$

In this way, the ratio between $K(f)$ and the so-called transduction function $T(f)$ is expressed as

$$\frac{K\left(f\right)}{T\left(f\right)} = \frac{Z_S - Z_I}{Z_S + Z_I} = \rho_1\left(f\right) \tag{11}$$

because $Z_I\left(f\right) = Z_I \in \mathbb{R}^*_+$ is the input impedance of the low-pass irregular analog filter in Fig. 8 and $\rho_1(f)$ is the reflection function [26]. Equating (11), $T(f) = E(f)/P(f)$ and $K(f) = F(f)/P(f)$, we have $\rho_1(f) = F(f)/E(f)$. From $F(f)$ and $E(f)$, the input impedance or admittances of the low-pass irregular analog filters between the terminations can be found, and the obtained circuit, showed in Fig. 8, can be obtained. For the low-pass irregular analog filter, the relation between the output impedance Z_L and the electric power system impedance Z_S, is expressed as [25]

$$Z_I = Z_S\frac{T(0) + K(0)}{T(0) - K(0)} = \frac{\sqrt{1+\varepsilon^2} + \varepsilon}{\sqrt{1+\varepsilon^2} - \varepsilon} = Z_L, \tag{12}$$

where $T(0)$ and $K(0)$ denote the values in which the transduction function for $\rho_1(0)$ offers the maximum power transfer (i.e., at $f = 0$). As both impedance Z_L and Z_S are connected at the output and input of the low-pass irregular analog filter, a double matched LC network with maximum power transfer is desired in the middle of the band-pass (e.g., f'_x). Notice that the input impedance of the low-pass irregular analog filter Z_I must be real and match with the electric power system impedance Z_S. Also, impedance matching with $Z_I = Z_S$ and, consequently, equals Z_L, provides the maximum power transfer. According to [37], we obtain

$$\frac{1}{\varepsilon} = \sqrt{\left(\frac{Z_L + Z_S}{Z_L - Z_S}\right)^2 - 1}. \tag{13}$$

A key limitation of this design is the relation between output impedance Z_L and electric power system impedance Z_S. Based on (13) it is straightforward to write

$$\left(\frac{Z_L + Z_S}{Z_L - Z_S}\right)^2 + 1 = \left(f^2 - 1\right)^4 \tag{14}$$

or

$$\frac{Z_L + Z_S}{Z_L - Z_S} = \sqrt{\left(f^2 - 1\right)^4 - 1}. \tag{15}$$

For the sake of simplicity, we have

$$\gamma = \sqrt{\left(f^2 - 1\right)^4 + 1}, \tag{16}$$

$$Z_L + Z_S = \gamma\left(Z_L - Z_S,\right) \tag{17}$$

and

$$Z_L = Z_S\frac{\gamma + 1}{\gamma - 1}. \tag{18}$$

The ratio between electric power system impedance Z_S and output impedance Z_L, in (18), defines the value of output and input impedance, respectively. When the constant $\gamma = \sqrt{2}$ applies, which represents -3 dB cut-off frequency, a ratio of $1 : 5.828$ is obtained. However, this ratio between the output impedance Z_L, which is fixed in $50\ \Omega$, and the electric power system impedance Z_S is not adequate because the value $1 : 5.828$ results in an input impedance of $Z_S = 8.579\ \Omega$, which

TABLE III: Values of the components of the low-pass irregular analog filter that were obtained using the Ladder software for $Z_L > Z_S$.

Component	Normalized value
L_1'	0.817421946071220
C_2'	0.865045016940072
L_2'	1.730090033879250
C_3'	0.40871097303582

TABLE IV: Values of the components of the low-pass irregular analog filter that were obtained using the Ladder software for $Z_S < Z_L$.

Component	Normalized value
C_6'	0.40871097303582
L_6'	1.730090033879250
C_7'	0.865045016940072
L_8'	0.817421946071220

is not a desired impedance value and outside the range of the desired access impedance value of electric power systems (i.e., between 25 Ω and 100 Ω, see [31]). In this sense, the low-pass irregular analog filter has been redesigned to obtain a ratio between electric power system impedance Z_S and output impedance Z_L equal to $1:2$ and $2:1$, as a consequence, to lock the input impedance of the low-pass irregular analog filter at 25 Ω and 100 Ω. According to (13), a new value of $\varepsilon = 0.353553390593$ is obtained, and the cut-off point of the low-pass irregular analog filter is applied to the new value $f_x = 1.6376$ Hz. The ratio between the output impedance Z_L and the electric power system impedance Z_S determines the edge frequencies of the low-pass irregular analog filter. It is given by

$$f_x = f_x' \sqrt{1 + \frac{1}{\sqrt{\varepsilon}}}. \tag{19}$$

To verify the validity of the redesigned low-pass irregular analog filter, a calculation was carried out with the HK software [38] when normalized values of Z_S and Z_L are considered (i.e., $Z_S = 2$ Ω and $Z_L = 1$ Ω). It resulted in $F(f) = \varepsilon(f^2+1)^2 = \varepsilon(f^4 + 2f + 1)$, $P(f) = 1$, $\varepsilon = 0.353553390593$, and $E(f) = \varepsilon(f^4 + 2.4467f^3 + 4.9932f^2 + 5.0950f + 3)$. Applying the Ladder software [38], we obtained the normalized values of the components of the low-pass irregular analog filter for $Z_L > Z_S$ as in Fig. 8(a). Applying a similar redesign procedure and $Z_S > Z_L$, we see that normalized values of components are equal to the previously designed low-pass irregular analog filter because both of them are a mirror of each other, see Fig. 8(b). The values of each normalized component evaluated by the Ladder software are listed in Table III for $Z_L > Z_S$ ($25 - 50$ Ω) and in Table IV for $Z_S > Z_L$ ($100 - 50$ Ω).

Finally, to obtain the real values of the normalized components, we need to apply the following equations:

$$L_n = 1.6376 \frac{Z_S L_n'}{2\pi f_c} \tag{20}$$

and

$$C_n = 1.6376 \frac{C_n'}{Z_S 2\pi f_c}, \tag{21}$$

where L_n' and C_n' is the normalized value of the inductor and capacitor, respectively, that are calculated by the HK and Ladder software, and $f_c \in \{50 \text{ MHz}, 100 \text{ MHz}, 500 \text{ MHz}\}$ is the cut-off frequency. The index n denotes the n^{th} inductor and capacitor of the low-pass irregular analog filter.

2) Low-pass Chebyshev analog filter: The choice of the low-pass Chebyshev analog filter for impedance matching with a $1:1$ ratio $Z_S = Z_L$ is based on the characteristics of access impedance of electric power systems detailed in [31]. Analyzing the Cumulative Density Function (CDF) of the access impedance reactance, we can see an inductive behavior of this reactance. Note that [31] showed an inductive behavior in 73% of the measured access impedance of electric power systems for the frequency band of $2-500$ MHz. Consequently, the aim is to design a low-pass analog filter with a series inductor that can help us deal with the reactance characteristic of access impedance in electric power systems.

According to simulations carried out in the Advanced Design System (ADS) software to design this analog filter, we can see that the first inductor, the component L_3 in Fig. 3, in the low-pass Chebyshev analog filter has a higher inductance value compared to the other analog filter structures, such as Elliptical, Butterworth, Gaussian, and Inverse Chebyshev. As a consequence, it facilitates the design of an impedance matching circuit. Based on [39], we can make the value L_3, which is a component of the low-pass Chebyshev analog filter, close to the reactance of the access impedance of electric power systems [31], and consequently, impedance matching improves. The analog filter consists of a Ladder network formed using series inductances and shunt capacitances (L_3, L_4, L_5, C_4, and C_5), see Fig. 3, for performing $50 - 50\Omega$ impedance matching. The values of each component evaluated by the ADS software are listed in Table I.

3) Scattering parameter analysis: Figs. 9, 10 and 11 show the magnitudes of the scattering parameters (i.e., reflection parameters, $S_{11}(f)$ and $S_{22}(f)$, and transmission parameters, $S_{12}(f)$ and $S_{21}(f)$) of the three analog filters, which were designed to constitute the prototype of the adaptive PLC coupling circuit, which covers the three frequency bandwidths. These magnitudes were obtained by using the software ADS.

The magnitudes that cover the frequency band of $2 - 50$ MHz, as shown in Figs. 9a and 9c, refer to the low-pass irregular analog filters with an input impedance of 25 Ω and 100 Ω, respectively, while Fig. 9b refers to the low-pass Chebyshev analog filter. Note that the magnitudes of $S_{12}(f)$ and $S_{21}(f)$ are around 0 dB. Also, the low-pass Chebyshev analog filter offers a better roll-off factor and a stop-band attenuation 11 dB higher than the low-pass irregular analog filters in 100 MHz. Concerning the magnitude of $S_{11}(f)$ and $S_{22}(f)$, we see that the low-pass irregular analog filters achieve a better impedance matching in the middle of the frequency band, see Figs. 9a and 9c. Also, the low-pass irregular analog filter with input impedance of 100 Ω, see Fig. 9c, shows the lowest magnitudes of $S_{11}(f)$ and $S_{22}(f)$ (e.g., -22 dB in 25 MHz and 36 MHz) while the low-pass Chebyshev analog filter achieves magnitude of $S_{11}(f)$ and $S_{22}(f)$ equal to -10 dB in 40 MHz. Magnitudes of $S_{11}(f)$ and $S_{22}(f)$ equal to -31 dB and -33 dB are observed

in 29 MHz and 48 MHz, respectively, when the low-pass Chebyshev analog filter is applied. Overall, the impedance matching for $100-50\ \Omega$ is the best while the worst is obtained for $25-50\ \Omega$.

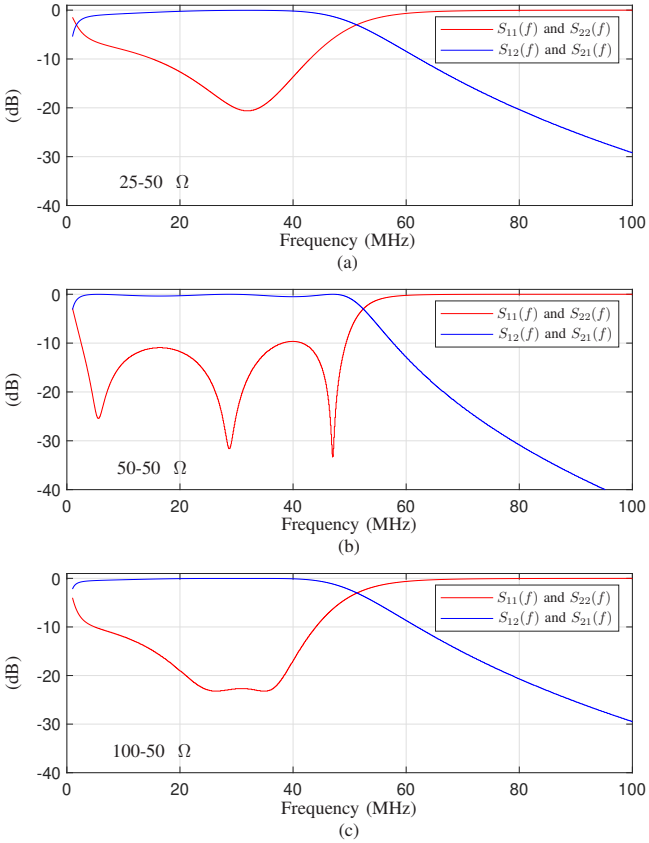

Fig. 9: Magnitude of the scattering parameter $S_{11}(f)$, $S_{22}(f)$, $S_{12}(f)$ and $S_{21}(f)$ of the analog filters designed for the adaptive PLC coupling circuit and the frequency band of $2-50$ MHz. (a) $25-50\ \Omega$, (b) $50-50\ \Omega$ and (c) $100-50\ \Omega$.

Regarding the frequency band of $2-100$ MHz, Figs. 10a and 10c show magnitudes of the scattering parameters of the low-pass irregular analog filters with an input impedance of 25 Ω and 100 Ω, respectively, while Fig. 10b shows the same magnitudes for the low-pass Chebyshev analog filter. All analog filters attain magnitude of $S_{12}(f)$ and $S_{21}(f)$ around 0 dB in the pass-band (i.e., $2-100$ MHz). For the entire stop-band, the low-pass Chebyshev analog filter offers a better roll-off factor and attains attenuation of 9 dB in the stop-band better than the others. Similarly, the low-pass irregular analog filters (Figs. 10a and 10c) attain a better impedance matching in the middle of the frequency band. Also, the low-pass irregular analog filter with input impedance of 100 Ω, see Fig. 10c, shows magnitudes of $S_{11}(f)$ and $S_{22}(f)$ as low as -32 dB in 62 MHz while the low-pass Chebyshev analog filter shows magnitudes of $S_{11}(f)$ and $S_{22}(f)$ equal to -10.5 dB in 62 MHz. For the frequencies 61 MHz and 100 MHz, the magnitudes of $S_{11}(f)$ and $S_{22}(f)$ of the low-pass Chebyshev analog filter are equal to -39 dB and -40 dB, respectively. Similarly, we can state that the impedance matching for $100-50\ \Omega$ is the best while the worst is obtained for $25-50\ \Omega$.

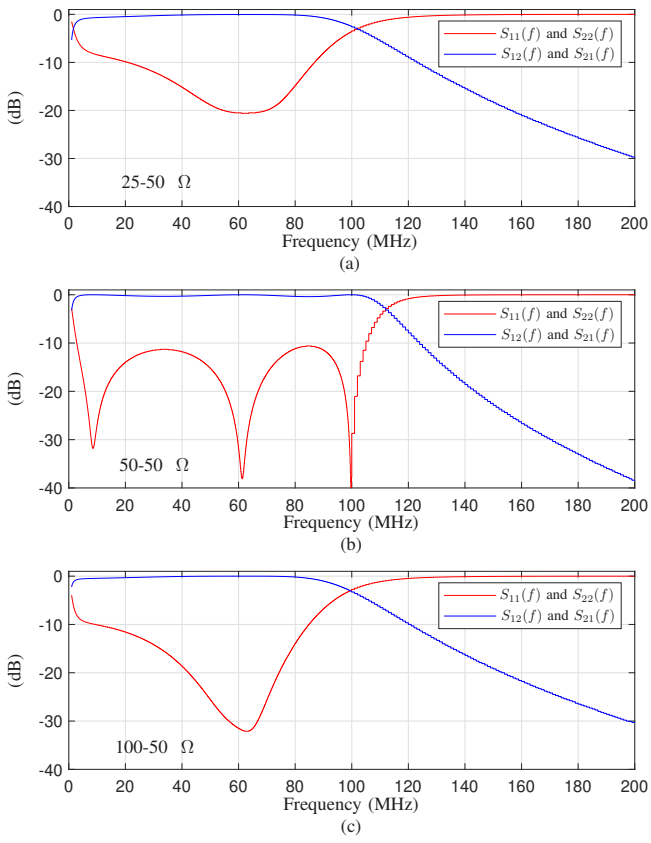

Fig. 10: Magnitude of the scattering parameter $S_{11}(f)$, $S_{22}(f)$, $S_{12}(f)$ and $S_{21}(f)$ of the analog filters designed for the adaptive PLC coupling circuit and the frequency band of $2-100$ MHz. (a) $25-50\ \Omega$, (b) $50-50\ \Omega$ and (c) $100-50\ \Omega$.

Focusing on the frequency band of $2-500$ MHz, Figs. 11a and 11c the magnitudes of scattering parameters of the low-pass irregular analog filters with the input impedance of 25 Ω and 100 Ω, respectively, while Fig. 11b shows the same magnitudes for the low-pass Chebyshev analog filter. Regarding the pass-band, we see that all analog filters attain magnitudes of $S_{12}(f)$ and $S_{21}(f)$ around 0 dB. Paying attention to pass-band, we see that the low-pass Chebyshev analog filter offers a better roll-off factor and attains attenuation 9 dB better than the low-pass irregular analog filters in 500 MHz. Also, the low-pass irregular analog filters with the input impedance of 100 Ω offer the worse stop-band attenuation (-28 dB) in 500 MHz. Analyzing the magnitude of $S_{11}(f)$ and $S_{22}(f)$, we see that the low-pass irregular analog filters (Figs. 11a and 11c) attain the best impedance matching in the middle of the frequency band. The low-pass irregular analog filters with input impedance of 25 Ω, Fig. 11a, attains the best magnitudes of $S_{11}(f)$ and $S_{22}(f)$ in 301 MHz (-29 dB), and the low-

pass Chebyshev analog filter showed the lowest magnitude of $S_{11}(f)$ (-9 dB in 450 MHz) and $S_{22}(f)$ (-56 dB in 302 MHz). The low-pass irregular analog filters with input impedance of 25 Ω, see Fig. 11c, shows the worse performance in terms of magnitude of $S_{11}(f)$ and $S_{22}(f)$, with -16 dB in 300 MHz. Again, we can state that impedance matching for $100-50$ Ω is the best while the worst is obtained for $25-50$ Ω.

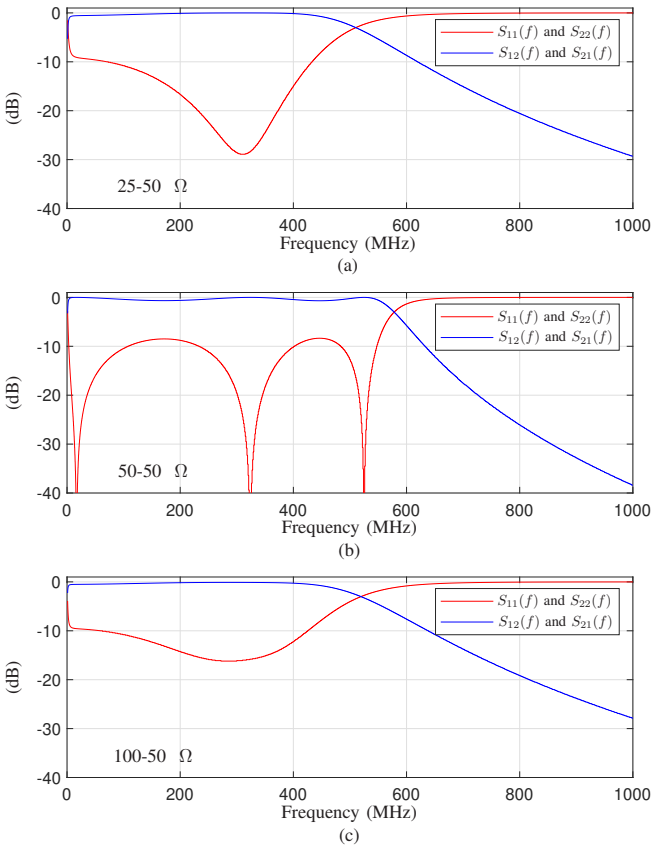

Fig. 11: Magnitude of the scattering parameter $S_{11}(f)$, $S_{22}(f)$, $S_{12}(f)$ and $S_{21}(f)$ of the analog filters designed for the adaptive PLC coupling circuit and the frequency band of $2-500$ MHz. (a) $25-50$ Ω, (b) $50-50$ Ω and (c) $100-50$ Ω.

D. Control unit

According to the Strategy #2, the analog filter yielding the best impedance matching between a PLC transceiver and electric power system is chosen by the control unit. Based on the voltage signal strength at the output of the impedance matching circuits bank, the control unit determines the Switch Bank position and chooses the impedance matching circuit.

The flowchart in Fig. 12 refers to the algorithm implemented in the control unit. The start point of the algorithm, when the adaptive PLC coupling circuit is connected to an electric power system, consists of switching the $M = 3$ impedance matching circuits, and the measured quantities are based on (7) because it informs the strength of the signal at the output of the Switch Bank #2. To reduce computational complexity, we used the average signal value (i.e., the average voltage value) in this implementation because it demands less computational complexity than the average power and consequently allows us to use a low-cost microcontroller.

For the sake of simplicity, from now on, the mean voltage level will be mentioned only as a voltage level. The voltage value for each impedance matching circuit is memorized, and the best circuit is selected as the one yielding the largest voltage level at the output impedance matching circuit bank. After that, the microcontroller selects the best circuit (analog low-pass filter). Following this first step, the microcontroller keeps checking the voltage level read by the analog-to-digital converter (ADC). If the voltage level drops significantly compared to with the best-stored levels, then a searching process for the best impedance matching circuit starts again, and it returns to the start point after a new choice is made. Furthermore, periodic searches are carried out, returning to the start point to ensure that the current impedance matching circuit is still the best.

1) Microcontroller: For controlling the switching of analog filters, a low-cost ESP-8266 microcontroller [40], which owns an integrated 10 bits ADC and general purpose input/output (GPIO) pins, is chosen. The microcontroller is attached to the connectors CN_1 and CN_2 and has three $LEDs$ (LED_1 to LED_3) to visually indicate the analog filter being used. Three GPIO connections are used to command each switch, and, as a consequence, the selection of the desired analog filter is carried out based on the knowledge of the voltage level, which is acquired by the ADC device.

2) Logarithmic amplifier: Fig. 13 shows the schematic of the chosen logarithmic amplifier (AD 8307) [41] for sensing the strength of the voltage signal at the output of the Switch Bank #2 when $N = 64$. The capacitors C_8 and C_9 and the inductor L_8 comprises a narrowband analog filter designed to detect the frequency of the maximum gain of the low-pass irregular analog filter and low-pass Chebyshev analog filter calculated by $(f_c/1.6376)$ [42], [43], where f_c is the cut-off frequency. The design of this band-pass analog filter was carried out using the ADS software. For instance, to design a 50 MHz band-pass analog filter for the adaptive PLC coupling circuit, the center frequency of the band-pass analog filter should be designed for 50 MHz/1.6376 = 30.53 MHz. Tab. V lists the values adopted for C_8, C_9 and L_8 components for each frequency band.

TABLE V: The values of components of the band-pass analog filter used by the AD 8307 device.

Frequency band (MHz)	Center frequency (MHz)	C_8 (pF)	C_9 (pF)	L_8 (nH)
$2-50$	30.53	47	33	1500
$2-100$	61.07	33	27	680
$2-500$	305.32	4.7	6.2	82

V. Performance Analysis

This section addresses performance analysis of the adaptive PLC coupling circuit that operates in the frequency bands of

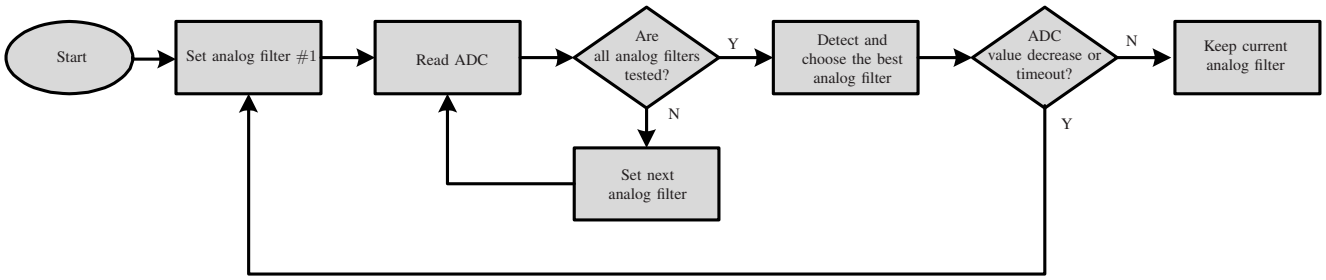

Fig. 12: Flowchart of the algorithm implemented in the Control Unit.

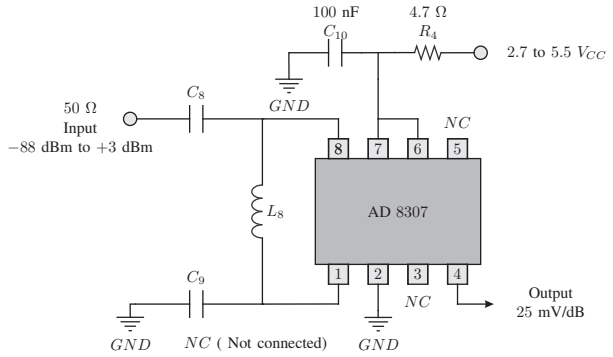

Fig. 13: Schematic of the chosen logarithmic amplifier AD 8307.

2-50 MHz, $2-100$ MHz, and $2-500$ MHz. The equipment used to carry out the analysis is the vector network analyzer (VNA) $N9912A$ Agilent, which frequency band ranges from 2 MHz up to 4 GHz [44]. For this purpose, the scattering parameters $S_{11}(f)$ and $S_{21}(f)$ of the adaptive PLC coupling circuit are compared to those obtained with the non-adaptive PLC coupling circuit, which has its input and output impedance equal to 50 Ω and makes use of a 5^{th} order elliptic analog filter to perform impedance matching. The scattering parameters $S_{21}(f)$ and $S_{11}(f)$ are obtained in terms of the 50 Ω impedance of the VNA [45].

A setup arrangement for measuring scattering parameters is shown in Fig. 14. The curves of the scattering parameters, which are measured between the adaptive PLC coupling circuits, were performed in a 127 V_{rms} 60 Hz electric power circuit with a power line of 15 meters in length and constituted by two parallel wires with 2.5 mm in diameter. The distance of 15 meters agrees with the distances observed in the average area of Brazilian apartments [46].

The measurement experiment was carried out using the following three setup arrangements:

- Setup #1: the use of the experimental setup with two the non-adaptive PLC coupling circuits with input and output impedance equal to 50 Ω, which will be called from now on as the non-adaptive PLC coupling circuit of 50 Ω. These coupling devices are connected to both sides of electric power systems.
- Setup #2: the use of the experimental setup with the non-adaptive PLC coupling circuit of 50 Ω, which is connected to one transceiver and an adaptive PLC coupling circuit (designed as a low-pass irregular analog filter and low-pass Chebyshev analog filter), which is connected to the other transceiver. The adaptive PLC coupling circuits own input impedance equal to 25 Ω, 50 Ω and 100 Ω and output impedance equal to 50 Ω. From now on, we will be called just as the adaptive PLC coupling circuit of 25 Ω, the adaptive PLC coupling circuit of 50 Ω or the adaptive PLC coupling circuit of 100 Ω, depending on which analog filter is selected.
- Setup #3: the use of the experimental setup with two adaptive PLC coupling circuits connected to both sides of electric power systems with the same input impedance (25 Ω with 25 Ω, 50 Ω with 50 Ω, and 100 Ω with 100 Ω) connected. Notice that the non-adaptive PLC coupling circuit of 50 Ω may present different curves from the adaptive PLC coupling circuit of 50 Ω, due to their different construction. The former uses an elliptic analog filter, while the latter applies a low-pass Chebyshev analog filter.

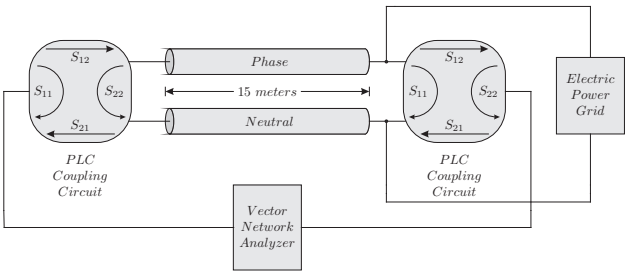

Fig. 14: The block diagram for the setup arrangement for measuring scattering parameters.

For the sake of simplicity, the following subsections highlight the measurement of $S_{11}(f)$ and $S_{21}(f)$ parameters using Setup #1, #2 and #3 for the frequency bands of $2-50$ MHz, $2-100$ MHz and $2-500$ MHz.

A. Comparison between Setup #1 and Setup #2 in terms of $S_{21}(f)$

This subsection presents a comparison of the magnitude of $S_{21}(f)$ when Setup #1 and Setup #2 are considered. In this sense, Figs. 15(a)-(c) show the magnitude of $S_{21}(f)$ for the frequency bands of $2-50$ MHz, $2-100$ MHz and $2-500$ MHz, respectively. The line with circle (○) markers refers to Setup #1 while the lines with triangle (△), diamond (◇) and square (□) markers are related to Setup #2 with the input impedance

of the adaptive PLC coupling circuit equal to 25 Ω, 50 Ω, and 100 Ω, respectively.

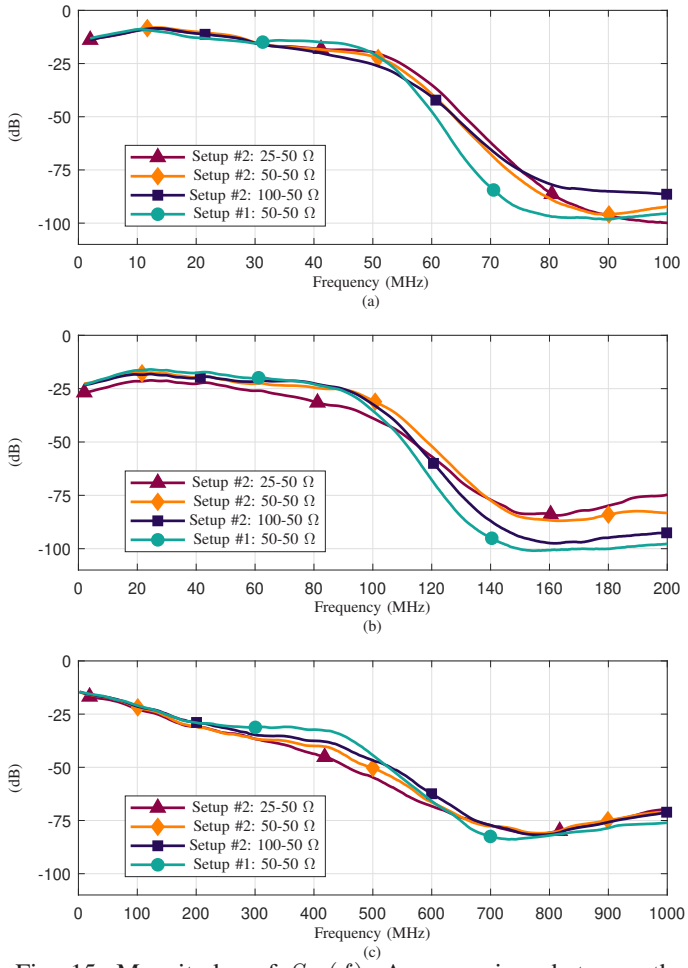

Fig. 15: Magnitudes of $S_{21}(f)$: A comparison between the adaptive PLC coupling circuit and the non-adaptive PLC coupling circuit of 50 Ω. (a) $2-50$ MHz, (b) $2-100$ MHz and (c) $2-500$ MHz.

In Fig. 15(a), we note that the behavior of the magnitudes of $S_{21}(f)$ up to 30 MHz are very similar, in both setups and their values vary between -8.5 and -15 dB. Analyzing the frequency from 30 MHz up to 50 MHz, the non-adaptive PLC coupling circuit of 50 Ω attained the lowest attenuation (line with ○ marks). Beyond the cut-off frequency of 50 MHz, we see a relatively sharp roll-off varying between -20 dB (line with △ marks) and -25 dB (line with □ marks). At the stop-band, the designed minimum attenuation of 40 dB is achieved, in the best case, at 58 MHz by the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) and, in the worst case, at 62 MHz by the adaptive PLC coupling circuit of 25 Ω (line with △ marks).

Fig. 15(b) shows that the adaptive PLC coupling circuit of 25 Ω yields the worst gain curve (line with △ marks) while the non-adaptive PLC coupling circuit of 50 Ω and the adaptive PLC coupling circuit of 50 Ω and 100 Ω show similar curves. The non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) attains the best insertion loss varying between -16 dB at the frequency of 22 MHz and -35 dB at the frequency of 100 MHz. The designed minimum attenuation at the stop-band of 40 dB is measured in 102 MHz for the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks). At the cut-off frequency of 100 MHz, we see a sharp roll-off varying between -30 dB and -39 dB and the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) presents the lowest attenuation.

Regarding the frequency of $2-500$ MHz, Fig. 15(c) shows that the magnitude of $S_{12}(f)$ varies between -15 dB at the frequency of 2 MHz and -53 dB at the frequency of 500 MHz. Also, it is clear that the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) offers the best insertion loss, varying between -15 dB at the frequency of 2 MHz and -45 dB at the frequency of 500 MHz. At the cut-off frequency of 500 MHz, the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) yields a sharp roll-off, which varies between -45 dB and -65 dB and provides the lowest attenuation. The adaptive PLC coupling circuits with input impedance equal to 25 and 50 Ω (lines with △ and ◇ marks, respectively) show the worst gain in the whole frequency band.

B. Comparison between Setup #1 and Setup #3 in terms of $S_{21}(f)$

The analysis of this subsection shows the results obtained from the measurements of the $S_{21}(f)$ parameter using Setup #3. The results achieved using Setup #1 are also presented for comparison purposes. Fig. 16(a), (b) and (c) depicts the measurement of the $S_{21}(f)$ scattering parameter comparing both setups at the frequency band of $2-50$ MHz, $2-100$ MHz and $2-500$ MHz, respectively. The line with ○ marks is the measurement acquired using Setup #1, while the lines with △, ◇ and □ marks are the measurements obtained using the Setup #3 with the input impedance of the adaptive PLC coupling circuits equal to 25 Ω, 50 Ω and 100 Ω, respectively.

Fig. 16(a) shows that, at the frequencies between 2 MHz and 15 MHz, the behavior of the magnitude of the scattering parameter of the non-adaptive PLC coupling circuit of 50 Ω and the adaptive PLC coupling circuits of 25 Ω, 50 Ω or 100 Ω are very similar. However, at the frequencies between 15 MHz and 40 MHz, the adaptive PLC coupling circuits of 50 Ω and 100 Ω (lines with ◇ and □ marks, respectively) have a better insertion loss varying between -9 dB and -14 dB in comparison with the non-adaptive PLC coupling circuit of 50 Ω and the adaptive PLC coupling circuit of 25 Ω. As can be seen, at the frequencies between 42 MHz and 50 MHz, the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) has the insertion loss with better gain and shows a better roll-off at transition band and attenuation at the stop-band frequency.

The results depicted by Fig. 16(b) shows that the adaptive PLC coupling circuits of 50 Ω and 100 Ω (lines with ◇ and □ marks, respectively) have better insertion loss compared to with the adaptive PLC coupling circuit of 25 Ω and the non-adaptive PLC coupling circuit of 50 Ω (lines with △ and ○ marks, respectively) at the frequency band 2 MHz up to 100 MHz. Moreover, the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) presents a better roll-off at transition band and attenuation at the stop-band frequency. The results

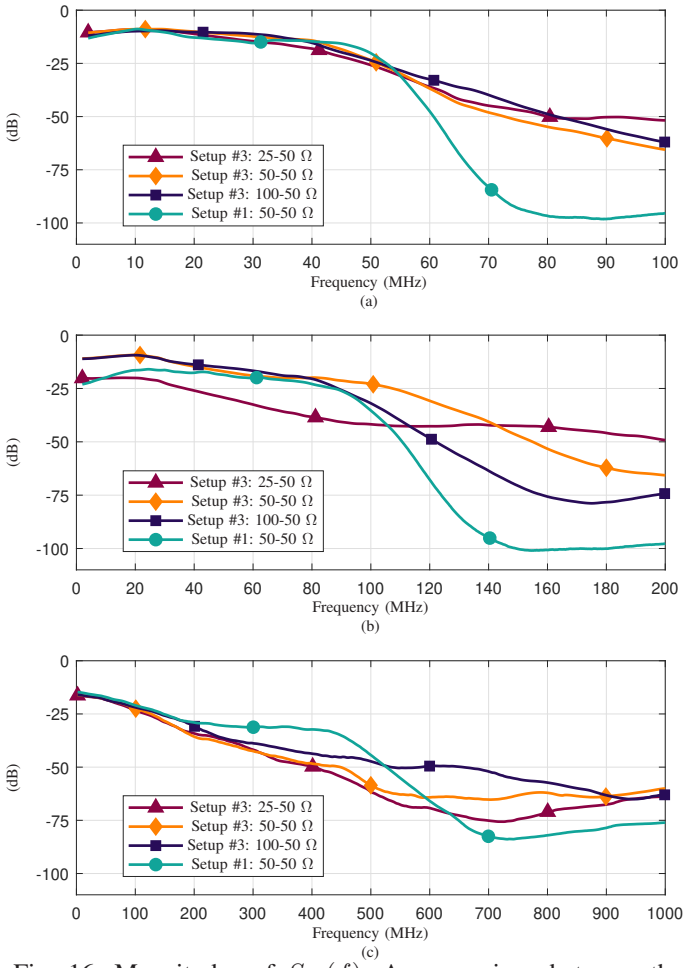

Fig. 16: Magnitudes of $S_{21}(f)$: A comparison between the adaptive PLC coupling circuit and non-adaptive PLC coupling circuit of 50 Ω. (a) $2-50$ MHz, (b) $2-100$ MHz and (c) $2-500$ MHz.

show that the adaptive PLC coupling circuit of 25 Ω (line with △) presents the worst results in all aspects, analyzing the band-pass, transition band and stop-band frequencies.

Finally, Fig. 16(c) depicts that the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) has a better insertion loss and attenuation at the stop-band frequency compared to with the adaptive PLC coupling circuits of 25 Ω, 50 Ω and 100 Ω (lines with , △, ◇ and □ marks, respectively). The adaptive PLC coupling circuit of 100 Ω (line with □ marks) has the second best results in terms of magnitude of the scattering parameter at the band-pass of 2 MHz up to 500 MHz and the adaptive PLC coupling circuits of 25 and 50 Ω (lines with △ and ◇ marks, respectively) show the worst results.

The previous subsections have shown that the inductive behavior of electric power systems causes higher attenuation in the magnitude of the scattering parameter of the non-adaptive PLC coupling circuit of 50 Ω and the adaptive PLC coupling circuits of 25 Ω, 50 Ω, and 100 Ω. Similar behaviors were noted in the results obtained with Setup #1 and Setup #3.

C. Comparison between Setup #1 and Setup #2 in terms of $S_{11}(f)$

This subsection presents the results obtained from the measurements of the return loss $S_{11}(f)$ parameter using Setup #2. The results achieved using Setup #1 are also shown for comparison purposes. Figs. 17(a)-(c) show the magnitudes of $S_{11}(f)$ related to both setups at the frequency bands of $2-50$ MHz, $2-100$ MHz, and $2-500$ MHz, respectively. The line with ○ marks is the measurement acquired using Setup #1. On the other hand, the lines with △, ◇ and □ marks are the measurements obtained using Setup #2 with the input impedance of the adaptive PLC coupling circuits equal to 25 Ω, 50 Ω and 100 Ω, respectively.

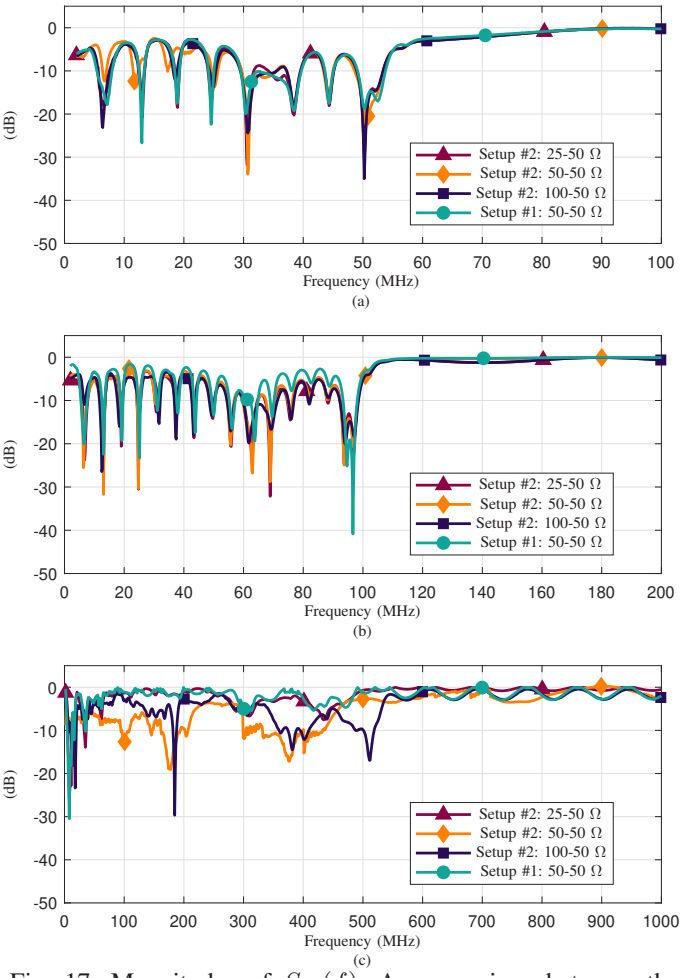

Fig. 17: Magnitudes of $S_{11}(f)$: A comparison between the adaptive PLC coupling circuit and the non-adaptive PLC coupling circuit of 50 Ω. (a) $2-50$ MHz, (b) $2-100$ MHz and (c) $2-500$ MHz.

The curves in Fig. 17(a) aims to show the magnitudes of $S_{11}(f)$. The ripples in the reflection coefficients range between -2.5 dB at the frequency of 15 MHz and -37 dB at the frequency of 50 MHz. We also observe that the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) presents the best impedance matching at the frequency of 30.5 MHz, which is the frequency designed to obtain the best impedance matching (50 MHz/1.6376), as discussed in Section IV-C. As a result,

it is found that the impedance matching is also noticed at different frequencies in the Fig. 17(a). At the frequency of 6 MHz, the adaptive PLC coupling circuit of 100 Ω (the line with □ marks) achieved a better impedance matching, equal to −23 dB, when compared to with the non-adaptive PLC coupling circuit of 50 Ω and the adaptive PLC coupling circuits of 25 Ω and 50 Ω. The same analysis can be noticed for the frequencies of 12 MHz and 24 MHz where the non-adaptive PLC coupling circuit of 50 Ω (the line with ○ marks) attained a good impedance matching. At the designed cut-off frequency, 50 MHz, the adaptive PLC coupling circuit of 100 Ω achieved a better impedance matching compared to the other PLC coupling circuits.

As well as in Figs. 17(a), Fig. 17(b) also presents a similar return loss $S_{11}(f)$ scattering parameter for all couplers analyzed, exhibiting ripples in the reflection coefficients. The ripples vary between −2 dB at the frequency of 22 MHz and −42 dB at the frequency of 98 MHz. We also observe that the adaptive PLC coupling circuit of 100 Ω (line with □ marks) has the best impedance matching, showing the best return loss $S_{11}(f)$ scattering parameter at the whole frequency band. At the frequency of 61 MHz, where the adaptive PLC coupling circuit of 25 Ω, 50 Ω and 100 Ω filters were designed to obtain the best impedance matching (100 MHz/1.6376), the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) attained the best result, as well as, at the frequencies of 7 MHz, 12 MHz, 22 MHz and 56 MHz. At the frequency of 98 MHz, near the designed cut-off frequency 100 MHz, the non-adaptive PLC coupling circuit of 50 Ω (the line with ○), attained the best impedance matching.

Interesting results can be observed analyzing the return loss in Fig. 17(c). The best impedance matching is obtained by the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) while the adaptive PLC coupling circuit of 25 Ω (line with △ marks) and the non-adaptive PLC coupling circuit of 50 Ω (line with ○ marks) show the worst impedance matching. The adaptive PLC coupling circuit of 100 Ω (lines with □ marks) shows a good impedance matching, equal to −30 dB at the frequencies 198 MHz and at the cut-off frequency and −17 dB at 505 MHz. As can be seen in Fig. 17(c), the impedance matching is not achieved at the frequency (500 MHz/1.6376) where the analog filters were designed to obtain the best impedance matching.

D. Comparison between Setup #1 and Setup #3 in terms of $S_{11}(f)$

This subsection presents the results obtained from the measurements of the return loss $S_{11}(f)$ scattering parameter using Setup #3. The results achieved using Setup #1 are also presented for comparison purposes. Figs. 18(a), (b) and (c) depict the measurement of the return loss $S_{11}(f)$ scattering parameter comparing both setups at the frequency bands of $2-50$ MHz, $2-100$ MHz and $2-500$ MHz, respectively. The line with ○ marks is the measurement acquired using Setup #1, while the lines with △, ◇ and □ marks are the measurements obtained using Setup #3 with the input impedance of the adaptive PLC coupling circuits equal to 25 Ω, 50 Ω and 100 Ω, respectively.

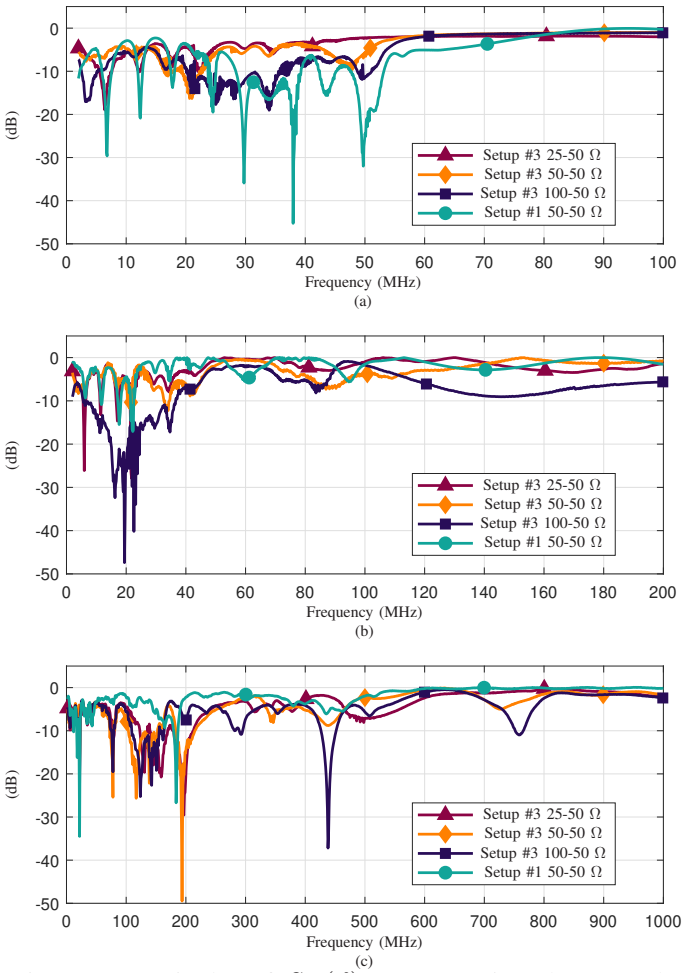

Fig. 18: Magnitudes of $S_{11}(f)$: A comparison between the adaptive PLC coupling circuit and the non-adaptive PLC coupling circuit of 50 Ω. (a) $2-50$ MHz, (b) $2-100$ MHz and (c) $2-500$ MHz.

As can be seen in Fig. 18(a), the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) and PLC coupling circuit of 25 Ω (line with △ marks) presented the worst impedance matching at the frequency between 23 MHz and 50 MHz. On the other hand, the adaptive PLC coupling circuit of 100 Ω (line with □ marks) shows the best impedance matching in the whole frequency band. The non-adaptive PLC coupling circuit of 50 Ω achieved the best impedance matching at the frequency of 38 MHz, equal to −45 dB and at the cut-off frequency 50 MHz, equal to −31 dB.

The results obtained in Fig. 18(b) shows that the adaptive PLC coupling circuit of 100 Ω (line with □ marks) attained the best impedance matching at the frequency band of 2 MHz until 82 MHz. However, the adaptive PLC coupling circuit of 50 Ω (line with ◇ marks) has the best impedance matching in the frequency between 82 MHz until 100 MHz. As can be seen between 50 MHz and 70 MHz, the values of the return loss $S_{11}(f)$ scattering parameter has the values near 0 dB which represents the total reflection of the $S_{11}(f)$ scattering parameter due to impedance mismatching between two PLC coupling circuits.

Based on Fig. 18(c), we can see that the best impedance matching is obtained by the adaptive PLC coupling circuit of $50\ \Omega$ (line with $\diamond$ marks). At the frequency of 199 MHz the value achieved, equal to -50 dB, is the best impedance matching in the whole band. The non-adaptive PLC coupling circuit of $50\ \Omega$ (line with $\circ$ marks) shows the worst impedance matching and the results of the adaptive PLC coupling circuit of $100\ \Omega$ (line with $\square$ marks) presents the impedance matching results near to the adaptive PLC coupling circuit of $50\ \Omega$ (line with $\diamond$ marks). According to Figs. 18(a), (b) and (c), the impedance matching designed for the low-pass irregular analog filter calculated for the frequencies (50 MHz/1.6376), (100 MHz/1.6376) and (500 MHz/1.6376) is not achieved in all PLC coupling circuits considered in the setups.

E. General Comments

The discussed results have shown that impedance matching circuits bank improve the power transfer between PLC transceivers and electric power systems when broadband PLC systems are considered; however, the dynamics of LV electric power systems make rather tricky to match the impedance accordingly at all times. Comparing the numerical results provided by the measurement setups, we note how difficult it is to match the impedance between two PLC coupling devices. Also, we have noticed that all magnitude curves are very similar to each other and for some frequencies, a good impedance matching can be attained. Overall, impedance matching using an adaptive PLC coupling circuit is challenging; however, it can offer improvement in comparison to the non-adaptive PLC coupling circuit. Furthermore, we have shown that the attenuation between PLC couplers can reach 60 dB in very specific and narrow frequency band in the pass-band. Also, the highest attenuation is observed at the upper frequencies of the pass-band, which agrees with the low-pass characteristic of electric power systems.

VI. Conclusion

This work has introduced theoretical justifications for using the analog filter bank approach to perform impedance matching between PLC transceivers and electric power systems. Based on the *principle of divide and conquer* together with the coherence time and the coherence bandwidth, we came up with two strategies for prototyping impedance matching circuits based on the analog filter bank approach when the time $\times$ frequency dynamics of access impedance in electric power systems are considered.

Based on experimental results, we have shown that the proposed analog filter bank approach offers better performance than usual. Also, we showed that the impedance matching between a PLC transceiver and an electric power system using the proposed analog filter bank approach is not a simple task to be accomplished. Moreover, impedance matching between two or more adaptive PLC coupling circuits may be a difficult task to be accomplished due to the coordination among them. It must be carefully addressed.

Overall, we have noticed that impedance matching based on the analog filter bank approach is an interesting research direction because there is room for remarkable improvements concerning the designs of analog filters and control unit.

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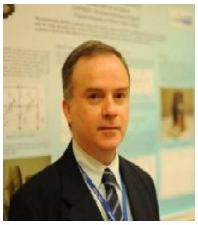

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